WL-TR-94-4086

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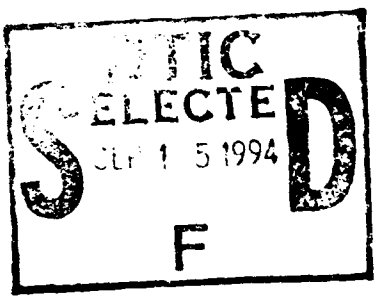
RELIABILITY WITHOUT HERMETICITY (RWOH) FOR INTEGRATED CIRCUITS (IC)



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March 1994

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Materials Directorate
Wright Laboratory
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13. ABSTRACT

This effort establishes baseline performance data for an inorganic (ceramic) protective coating over integrated circuits in plastic packages. Severe and differentiating environmental stress testing demonstrated protection against humidity beginning to approach the protection offered by hermetic packaging. Advantages in size and weight are inherent in the technology.

14. SUBJECT TERMS

Reliability Without Hermeticity (RWOH), Reliability of Electronics, Silicon Carbide, Electronics Packaging.

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DOW CORNING

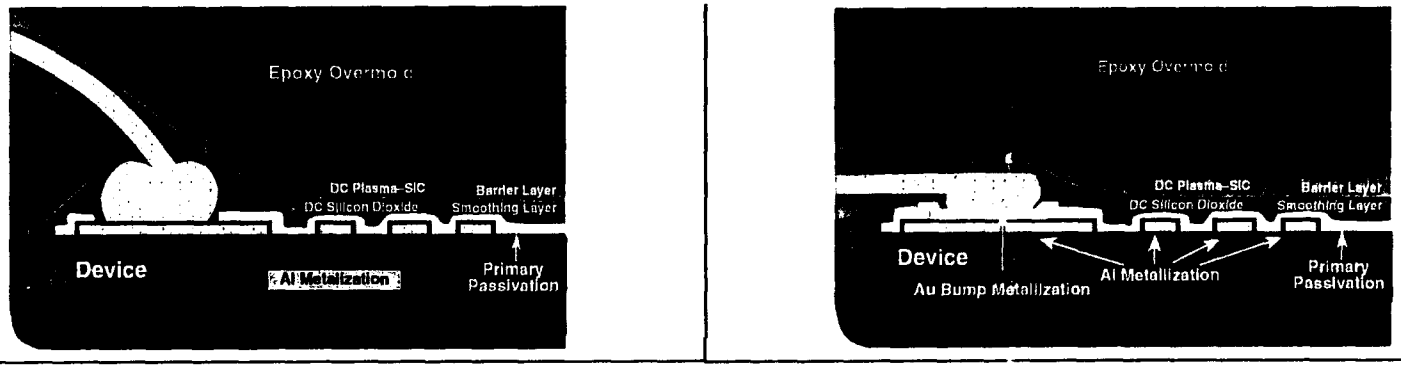
National Semiconductor

Reliability Without Hermeticity

Contract No: F33615-90-C-5009

Objective: Demonstrate the improved reliability of plastic packaged ICs using Dow Corning's Ceramic Coating Technology to provide a moisture/ion barrier on National Semiconductor's plastic encapsulated ICs.

Sealed Chip in a Plastic Package



Conclusions:

- Ceramic Coating Materials and Processes Do Not Degrade IC Performance in Assembly, 168 Hr. Burn-in, SMT Assembly, or Extended Temperature Cycling (+150 to -65°C), Autoclave (121°C), and HAST (159°C) Exposures.
- Device Preconditioning (24 Hrs. Autoclave Followed by 200 Temp. Cycles) Accelerates the Time to Failure by 100% in HAST Exposure of Plastic Packaged CMOS Devices.
- Reliability Differentiation In HAST @ 159°C Was Achieved Between Ceramic Coated and Standard Die in Plastic Packages. Protection of ICs From Moisture and Mobile Ions Using Thin-Film Ceramics Significantly Increased Device Lifetimes (3X).
- Reliability Differentiation In HAST @ 140°C Was Not Achieved On TapePak™ or PDIP Test Devices (1100 Hrs).
- Reliability Differentiation in Autoclave, HAST, and Temp. Cycling/Salt Fog Exposures Was Consistently Achieved Between Ceramic Coated and Standard Die in Ceramic Side-Brazed, Unlidded Chip Carriers With Aluminum Wire.
- Ceramic Coated Leadwires Unprotected from Mechanical Shock and Vibration are Susceptible to Fracture At High Stress Regions (Neckdown to Frame).
- Future Development of Thin-Film Ceramic Coatings For Improving the Reliability of Bare Die Is Directed At The Wafer Level For Low Cost *Dual Use* Advance Packaging Applications.

PREFACE

This final technical report describes the results obtained during 2.5 years of contract effort on the Wright Laboratories (WL) sponsored program "Reliability Without Hermeticity for Integrated Circuits." The objective of the Air Force RWOH program is:

> To evaluate the industry's most promising integrated circuit coating material for application in military systems. Testing and failure analysis data will be used to determine if non-hermetic integrated circuit packaging approaches appear feasible to replace standard hermetic packaging currently used in military systems. This program is to provide assessment data of integrated circuits in single chip packages. This data should establish the baseline technology directions for the eventual coating of multichip packages."

Specifically, this program will evaluate state-of-the-art plastic package reliability and an advanced inorganic (ceramic) protective coating system that will allow replacement of hermetic packages in commercial and military products. The goals of this contract effort are to establish baseline performance data on plastic packaged ICs, integrate the inorganic protective coatings into existing IC plastic packaging, and assess their performance through severe and differentiating environmental stress exposures. Captain Robert Frigo, USAF WL-MLSA, was the Program Manager for the RWOH program.

National Semiconductor Corporation (NSC) is the prime contractor for this program under Contract F33615-90-C-5009; Mr. Eric Huang was the Principal Investigator of NSC efforts to integrate new advanced thin film packaging technologies with NSC's existing TAB processes and packaging technologies. Dow Corning Corporation (DCC), under subcontract to NSC, focused its efforts on the development of low-temperature thin film inorganic dielectric materials (ceramic coatings) which has shown application in providing an advance packaging technology for IC protection. Mr. Robert Camilletti was the Principal Investigator for DCC efforts described in this report.

The tasks defined for Contract F33615-90-C-5009, the organizational responsibilities, and task sponsorship are:

Task 1.	Definition of Reliability Test Program (WL/NSC/DCC) Contract funded
Task 2.	Engineering Studies (DCC) Dow Corning funded
Task 3.	Leadframe Strip Coating Process (DCC) Contract funded
Task 4.	Assembly of Test Samples and Control Samples (NSC) Contract funded
Task 5.	Coating of Test Samples with Two Ceramic Layers (DCC) Contract funded
Task 6.	Overmold Test Samples (NSC) Contract funded
Task 7.	Reliability Testing of Coated CMOS Integrated Circuits (DCC); Dow Corning funded
Task 8.	Reliability Testing of Coated Operational Amplifier Integrated Circuits (NSC); Contract funded
Task 9.	Failure Analysis (DCC/NSC) Dow Corning/NSC funded
Task 10.	Reports (DCC/NSC) Contract funded

By mutual agreement, technical results of both contract funded and Dow Corning funded efforts are being reported. However, under this agreement, dissemination of results from Dow Corning funded efforts is restricted under DFARS 252.227-7013.

National Semiconductor personnel under contract support that directly contributed to the results of this program were:

Robert Byrne	Program Manager; Contracts
Eric Huang	Principal Investigator
John Jackson	Packaging Manager
Edwin Slipher	Quality Assurance and Reliability Staff Mgr.
Mark Baker	TAB/ Bump Fabrication Packaging Engineer
Howard Allen	Packaging Engineer South Portland

Dow Corning personnel under contract support that directly contributed to the results of this program are:

Clay Bearinger	Application Dev., Reliability Testing
Robert Camilletti	Principal Investigator
Grish Chandra	Program Manager; Electronics
Fred Dall	Electrical Characterization
Diana Dunn	Application Development
Mark Loboda	Thin Film Char., PECVD, a-SiC:H
Jeff Seifferly	Deposition Development

The investigators wish to acknowledge the technical assistance provided by Mr. David Ross and Mr. James Reilly of Rome Laboratory.

Principal Investigators

Eric Huang
National Semiconductor Corp.

Robert C. Camilletti
Dow Corning Corp.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

GLOSSARY OF TERMS

AES	Auger electron spectroscopy
AFS	Atomic fluorescence spectroscopy
BP	Bond pad
CMOS	Complementary Metal Oxide Semiconductor
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
D-packages	Ceramic sidebrazed cavity package
DCC	Dow Corning Corporation
DoD	Department of Defense
DI	Deionized (water)
DIP	Dual In-line Package
EDS	Electron dispersive X-ray spectroscopy
EOS	Electrical overstress
ESD	Electrostatic discharge
EMC	Epoxy molding compound
FP	Frame post
FTIR	Fourier transform infrared spectroscopy
GC	Gas chromatography
HAST	Highly Accelerated Stress Testing
HIPEC Q2-1345	Dow Corning™ dimethylsiloxane cyclics
I/O	Input/Output
IC	Integrated Circuit
ICE	Integrated Circuit Engineering
ILB	Inner lead bond
IPA	Isopropyl alcohol
IR	Infrared
JEDEC	Joint Electronic Device Engineering Council
JIT	Just-in-time
Me	Methyl group, CH_3
MCM	Multichip Module
NMR	Nuclear magnetic resonance
NSC	National Semiconductor Corporation
NSWC	Naval Surface Warfare Center
OLB	Outer lead bond

Op-Amp	Operational amplifier
ORS	Oneida Research Services
OM	Optical microscopy
PDIP	Plastic Dual In-line Package
PECVD	Plasma enhanced chemical vapor deposition
PED	Plastic encapsulated devices
PLCC	Plastic leaded chip carrier
ppm	Parts/million
ppb	Parts/billion
PQFP	Plastic quad flat pack
PTFE	Polytetrafluoroethylene
r	Correlation coefficient
RF	Radio Frequency
RH	Relative Humidity
RL	Rome Laboratory
RWOH	Reliability without Hermeticity
SAM	Scanning acoustic microscopy
SCB	Silacyclobutane, a-SiC:H precursor
SCCM	Standard cubic centimeters
SEM	Scanning electron microscopy
SiC	Silicon carbide
SiN	Silicon nitride
SiO_2	Silicon dioxide
SMT	Surface mount technology
SPEC	Surface Protected Electronic Circuits
TAB	Tape automated bonding
T_g	Glass transition temperature
TGA	Thermogravimetric analysis
TMA	Thermomechanical analysis
UVOCS	UV / ozone cleaning system
XPS	X-ray photoelectron spectroscopy
WL	Wright Laboratory
WPAFB	Wright-Patterson Air Force Base

EXECUTIVE SUMMARY

The reliability of state-of-the-art commercial plastic packaging and inorganic (ceramic) coating technologies were assessed using severe and differentiating environmental exposures that would allow the replacement of hermetic packages in commercial and military products. The reliability data was evaluated using Weibull analysis, which revealed that the reliability of commercial plastic encapsulated devices can be improved by at least one order of magnitude when the die are coated with thin-film ceramic coatings prior to plastic molding. This combination of ceramic coatings with conventional plastic packaging provides reliability that begins to approach that of hermetic packages.

Background

Traditional plastic packaging has not been adequate for the rigorous demands of the military environment. Recent advances in materials, processes, and package technologies have prompted new investigations to assess their reliability. This study evaluates the comparative effectiveness of protective inorganic (ceramic) coatings in state-of-the-art plastic packages under extreme and differentiating environmental exposures.

Throughout the development of the integrated circuit, studies have repeatedly identified ionic contamination and moisture as major contributors to device failure. One of the primary sources of ionic contamination in commercial plastic packaging has been the epoxy molding compounds (EMCs). These materials also have intrinsic high water vapor permeability and absorptivity, which permit the diffusion of reactive ions to the circuit elements, and can corrode the circuit metallization. Stepwise improvements of EMCs have enhanced the reliability of plastic encapsulated devices, but issues regarding the long term storage and reliability of these devices have not been adequately addressed for military products.

This report presents the results of a Wright Laboratory Manufacturing Technology (ManTech) program undertaken to integrate the protective ceramic coating technology into existing IC plastic packaging and assess the reliability of state-of-the-art commercial plastic packaging technologies through severe and differentiating environmental exposures. Baseline and comparative reliability data on these packaging technologies are made against traditional hermetic packaging.

Additionally, the comparative effectiveness on the reliability of bare die assembled in ceramic chip carriers are assessed for insertion into MCM applications.

For this study, the NSC LM124 operational amplifier (Op-Amp) and the NSC '011B CMOS integrated circuits were selected as test vehicles due to their ent sensitivity to mechanical stress, moisture ingress, and ionic contamination. These test vehicles/devices were assembled using best commercial practices in plastic dual inline packages and plastic quad flat packs, commercially known as TapePak™. The ceramic coatings consist of two inorganic layers; the first is a silicon dioxide layer for smoothing of the circuit topology, the second is an amorphous hydrogenated silicon carbide (plasma-SiC) layer which is a barrier against the ingress of moisture and ions. This study integrated these thin-film ceramic coatings on partially assembled integrated circuits mounted on chip carriers prior to plastic overmolding to produce a sealed chip with enhanced reliability.

Experimental

Application and characterization of the thin-film ceramic coatings to partially assembled integrated circuits mounted on chip carriers was the primary focus of the experimental effort. Surface preparation techniques were investigated to assure the highest possible coating integrity and sealing properties of the circuit substrate and I/0 interconnect.

Hydrogen silsesquioxane was the chemical precursor for the silicon dioxide layer, while silacyclobutane (SCB) was the precursor for the amorphous hydrogenated silicon carbide (plasma-SiC) layer. Advances in chemical precursor technology were dependent upon the development and refinement of chemical formulas and characterization techniques. Procedures were developed for measuring pinhole density, film density, and substrate adhesion of thin films.

Application techniques for the solution applied silicon dioxide smoothing layer to a leadframe chip carrier were assessed. The use of ultrasonic spray application provided uniform coverage on the circuit assembly. The remaining processes used in applying the ceramic coatings were derivations of standard semiconductor fabrication techniques which were tailored to leadframe applications. Typical thicknesses of the

applied films were 200-300 nm for the silicon dioxide and 600-700 nm for the plasma-SiC layers.

The intrinsic mechanical stresses in the deposited ceramic coatings and the adhesion of commercial EMCs to the plasma-SiC were investigated. A single layer silicon dioxide coating is under tensile stress; the plasma-SiC barrier layer is under a relatively small compressive stress. This stress becomes slightly more compressive upon the first 100 temperature cycles (-65 to 150°C). The behavior of the dual-layer coating mimics the carbide layer by itself. These results indicate the silicon dioxide/plasma-SiC coatings are relatively insensitive to temperature cycling.

Adequate adhesion between the ceramic coatings and the EMC was assessed and compared to standard commercial packaged devices. SEM cross-sectioning and scanning acoustic microscopy showed good adhesion of the EMC to the plasma-SiC barrier layer, and between the silicon dioxide and the existing plasma-SiN primary passivation regardless of whether the devices were exposed to autoclave or temperature cycling conditions.

A single lot of each device type, mounted on chip carriers, was divided into two groups; one group was coated with SiO_2/plasma-SiC at 250°C, the other group remained standard (uncoated) commercial devices. Characterization on a representative sampling of coated die included coverage and sealing of the aluminum bond pads using the MIL-STD-883 glassivation test and bond pull strength tests. Coated die were unaffected after 15 hours of exposure to the glassivation acid solution. The bond pull strength of coated CD4011B devices on leadframes with gold wire was found to be slightly reduced, from 13 to 12 grams, when compared to standard (uncoated) devices. Coated CD4011B devices in ceramic sidebrazed packages (D-packages) with aluminum wire had a reduction in bond pull strength from 10 grams to 6 grams when compared to standard (uncoated) devices. The bond pull strength was far above the minimum requirement of 2 grams.

CD4011B and LM124 devices, both ceramic-coated die and standard uncoated die were transfer molded in epoxy (Nitto MP101S and Sumitomo 6300 respectively) using standard processes employed by NSC. Lead trim and form, solder dip, and marking was completed. High electrical yields (99%) were achieved on the ceramic-coated devices; equal to the standard commercial devices. These test devices will be

referred to as coated or standard PDIPs, D-packages, and TapePaks™ respectively.

A variety of severe and differentiating environmental exposures were used to assess the reliability of commercial state-of-the-art plastic packaged devices for military products. Well understood and robust devices, CD4011B CMOS and LM124 Op-Amp, were packaged in PDIP and TapePak™ technologies using standard commercial practices. Ceramic-coated die were integrated into existing commercial plastic packaging, subjected to environmental exposures, and assessed with respect to standard (uncoated) commercial devices. Reliability tests were also performed comparing ceramic-coated die in plastic packages with standard die in traditional hermetic packages. Additionally, the reliability of ceramic-coated CD4011B bare die in chip carriers was assessed with respect to standard die for correlation with future MCM insertion.

Initially, the reliability of coated CD4011B devices, both PDIPs and D-packages, against standard commercial devices was assessed under several test regimes. Specific environmental stress tests which provided reliability differentiation were then used in subsequent testing with the LM124 Op-Amp. A detailed description of the environmental test conditions used on the CD4011B devices is listed below.

Autoclave	JEDEC-STD No. 22B, Method A102-A (121°C, 100% RH, 1 ATMG)
HAST:	JEDEC-STD No. 22, Method A110 (157±2°C, 85% RH, 4 ATMG, 10 V)
Temp Cycle:	MIL-STD-883D, Method 1010.7, Test Condition C (-65 to +150°C, 1 hr per cycle)
Salt Fog:	MIL-STD-883D, Method 1009.8, Test Condition A (35°C, 0.5% NaCl, inclined 15° from normal)

To achieve a closer approximation to service-related performance conditions of the CMOS devices, a parallel reliability test scheme was devised by splitting each device configuration into two groups; one group (Sequence A) was exposed directly to environmental testing while the second group (Sequence B) was preconditioned immediately before environmental exposure to provide sequential reliability data. Sequential testing combines moisture (absorption, ingress) with mechanical stresses (thermal, flexure, fatigue, and vibration). The reliability testing for the CD4011B CMOS

device is shown schematically in Figure 1.

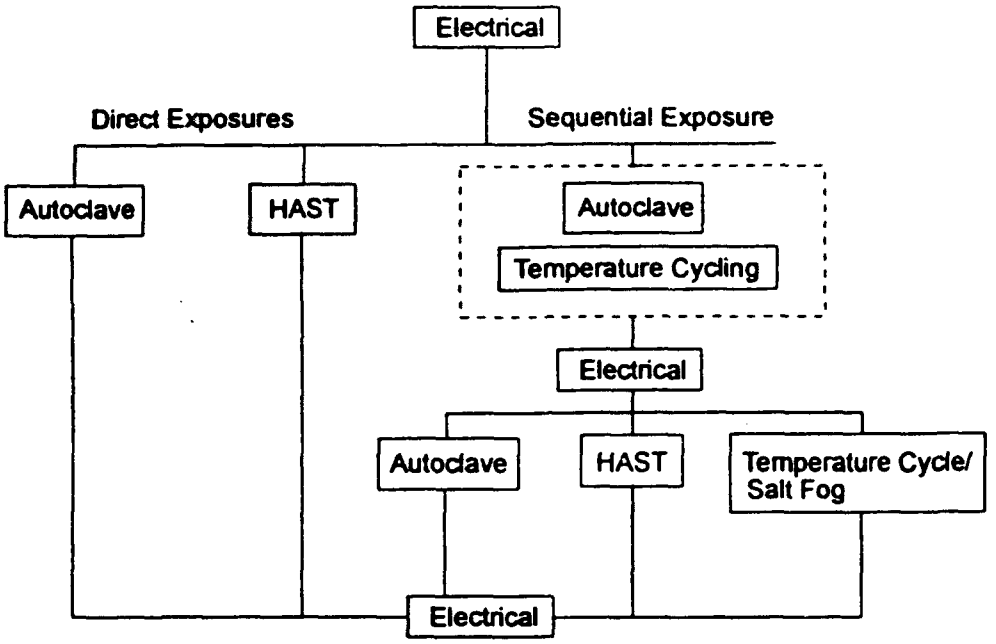


Figure 1. Summary of Reliability Test Program

Statistical quantities of CMOS devices were subjected to preconditioning exposure which consisted of 24 hours of autoclave (121°C, 100%RH, 1 atmg) followed by 200 temperature cycles (-65 to +150°C). Devices passing the preconditioning exposure and a lot of unconditioned devices were subdivided and subsequently subjected to either autoclave, HAST, or temperature cycling/salt fog for sequential or direct reliability testing respectively. All devices were randomly selected for environmental testing. At the prescribed intervals, the devices were removed from the chamber and allowed to set in a nitrogen purge desiccator for 24 hours prior to full electrical testing. Device failures were defined as an open circuit, short, or irreversible parametric shift attributable to ion or moisture induced circuit degradation. Examples of conditions not considered failures include electrostatic discharge (ESD), electrical overstress (EOS), package related leakage current, board assembly (solder) degradation, etc.

The performance results from the electrical (parametric) testing on all package

configurations were tabulated. The results from the CD4011B reliability testing will be presented by first, comparing the reliability and failure analysis of standard commercial die (no die coat) in plastic packages against ceramic-coated die in plastic along with the hermetic control group, and secondly by comparing the reliability and failure analysis of standard bare die (no die coat) in D-packages tested with no lid against ceramic-coated die in similar packages.

CD4011B CMOS in Plastic and Hermetic Packages

No significant difference in reliability data was found between direct and sequential autoclave exposure. The reliability of ceramic-coated PDIPs was equal to that of standard commercial PDIPs and hermetic packaged devices in sequential autoclave and temperature cycle/salt fog exposures. No package differentiation was achieved as a result of either 1000 hours of sequential autoclave or 1000 cycles of sequential temperature cycling/salt fog.

HAST exposure clearly differentiated the level of CD4011B reliability provided by each packaging system. Reliability results from direct and sequential HAST exposure at 159°C (Sequence A and B respectively) clearly indicate that the use of low temperature thin-film ceramic-coatings improved the time-to-first-failure and the mean-time-to-failure of standard die in plastic packages by at least a factor of two. The time-to-first-failure increased from 300 to 900 hours in direct HAST exposure and from 300 to 600 hours in sequential HAST exposure as compared to standard PDIPs. The mean-time-to-failure increased from 676 to 1192 hours in direct HAST exposure and from 544 to 1392 hours in sequential HAST exposure as compared to standard PDIPs. Comparative reliability data shown in Figure 2 illustrates that the reliability of coated PDIPs begin to approach that of hermetic packaging. Sequential HAST exposure decreased the mean-time-to-failure of standard and coated PDIPs by 100 hours when compared to the results derived from direct HAST exposure.

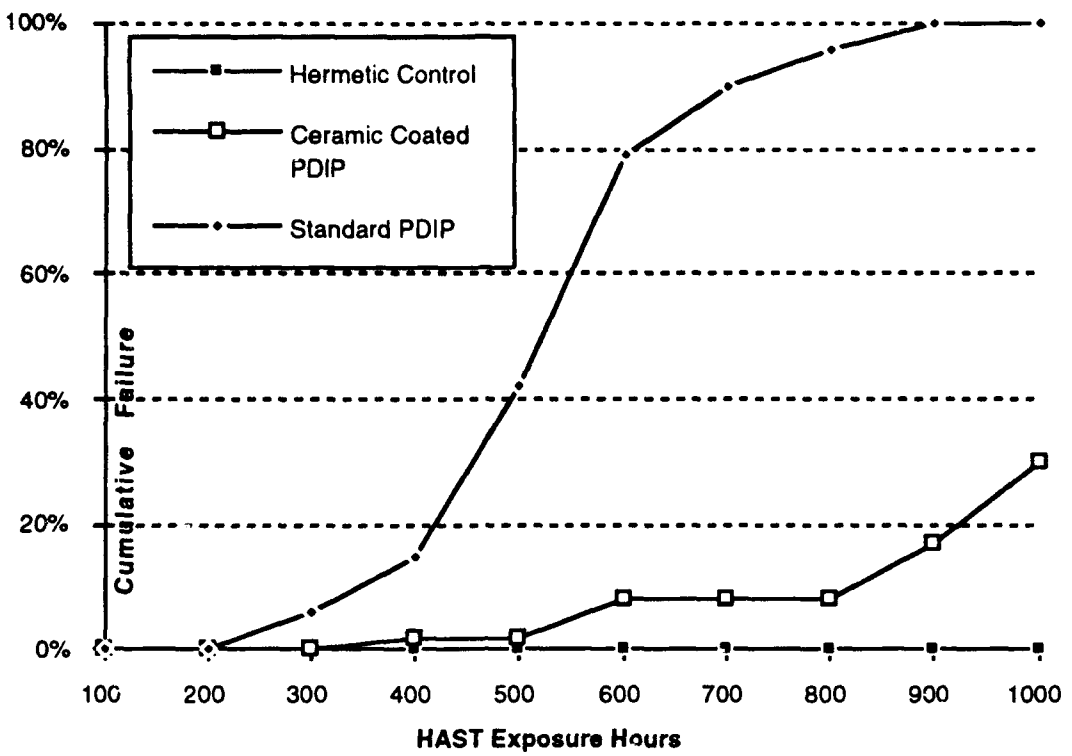


Figure 2. Sequential HAST Reliability Results on CD4011B CMOS Devices.

Evaluation of the plastic package reliability data by Weibull analysis reveal at least a one order of magnitude decrease in failure rate when the bare die are protected with the ceramic coatings. This is however the worst case evaluation for the coated PDIPs since significantly different failure mechanisms, not related to this study, were identified.

Analysis of representative CMOS devices which failed HAST exposure was performed by Oneida Research Services. Standard PDIPs failed from multiple open circuits due to severe, classical corrosion of the biased bond pads. The failures of the ceramic coated PDIPs, prior to 800 hours of HAST, appear to be caused by non-classical failure mechanisms which are not completely understood. These mechanisms include 1) catastrophic dissolution of all aluminum bond pads with, for some die, complete dissolution of ground and output circuit traces; 2) corrosion of

floating output bond pads; 3) anodic dissolution of gold ball bonds ; and 4) electrical current overstress. Beyond 800 hours, classical aluminum bond pad corrosion was observed along with non-classical mechanisms. Hermetic control device failures were due to electrical current overstress which are considered non-classical failure mechanisms not related to this study.

An analysis of randomly selected functional CMOS devices exposed to 1000 hours of sequential HAST at 159°C revealed that both coated PDIPs and hermetic package controls exhibited minor classical bond pad corrosion at biased (V^+) inputs. No standard PDIPs survived 1000 hours of sequential HAST.

The application of the ceramic coatings did not adversely affect the electrical performance of the integrated circuit even after 1000 hours of sequential reliability testing. The data suggest that the preconditioning exposure used in sequential testing accelerated device degradation with no change in failure mode. These data also suggest that the ceramic coatings are compatible with present state-of-the-art semiconductor passivation materials (approx. 400°C) and back-end assembly processes.

CD4011B CMOS in Ceramic Side-Brazed Packages (D-packages)

The reliability of bare CMOS devices in ceramic chip carriers was assessed for correlation with future MCM insertion. These bare die, assembled in open cavity sidebrazed packages (D-packages), were subjected to all of the environmental stress exposures without lids.

Significant performance differentiation between standard commercial and ceramic-coated die was obtained immediately from preconditioning exposure. Direct or sequential testing in autoclave, HAST, and temperature cycling/salt fog exposures clearly indicates that the reliability of coated D-packages far exceeds that of standard D-packages. Differentiation between standard and coated D-packages was achieved after 100 hours of autoclave and HAST, and after 3 hours of salt fog exposures. A significant improvement in moisture and ion protection was obtained using the ceramic coatings. No die related failures were observed on ceramic-coated die during the reliability testing. Single-point leadwire corrosion at the neckdown to frame post region was the dominant failure mechanism of coated D-packages.

In summary, the reliability of CMOS test devices was significantly improved by the use of the low-temperature ceramic coatings. The materials and processes used for depositing the ceramic coatings did not adversely affect the function of the CMOS devices even after 1000 hours of environmental stress tests. Only ceramic-coated devices consistently survived 1000 hours of direct and sequential reliability testing. Ceramic-coated leadwires unprotected from mechanical shock and vibration are susceptible to fracture at high-stress regions (neckdown to bond pad or frame post). Analyses of fully functional ceramic-coated devices (coated D-packages) surviving 1000 hours of environmental exposure revealed that multilayer ceramic coatings protect the circuits from moisture and mobile ions.

The reliability test results generated on the standard commercial CD4011B CMOS PDIPs indicated that the HAST exposure was the most differentiating environmental test used so far in this study. Neither 1000 hours of autoclave nor 1000 temperature cycles followed by 24 hours of salt fog provided adequate package differentiation, regardless of whether the devices had undergone a preconditioning exposure. HAST, on the other hand, did induce both ion and moisture related failure mechanisms on the CMOS devices and would be the appropriate test condition for the LM124 Op-Amp.

LM124 Op-Amp in TapePak™, PDIP and Hermetic Packages

Statistical quantities of Op-Amp devices were subjected to preconditioning exposure which consisted of 168 hours of 125°C burn-in, 40 seconds of vapor phase reflow exposure at 219°C, and 200 temperature cycles at -65 to 150°C. The purpose of this preconditioning is to simulate the manufacture, storage, and assembly processing of military-grade SMT devices. After preconditioning exposure, the LM124 test vehicles were subjected to 1100 hours of HAST exposure at 140°C. Significant quantities of standard commercial and ceramic-coated TapePak™ devices failed electrical testing after 100 hours of exposure. Electrical failures of standard commercial PDIPs or hermetic controls were not observed until 900 hours of exposure.

Analysis of representative Op-Amp devices which failed HAST exposure revealed that only one device was found to have exhibited a corrosion or moisture related failure, a standard commercial PDIP. The significant quantity of electrical failures was determined to be caused by failure of the conversion board used both inside the HAST chamber for biasing surface mount devices (TapePak™) and for room

temperature electrical testing. Aside from that part, no additional device failures were detected through 1100 hours of HAST at 140°C.

In summary, sequential HAST exposure at 140°C did not differentiate between the package configurations used in this study for the LM124 Op-Amp. These data indicate that the reliability of ceramic-coated TapePaks™ and PDIPs was equal to that of standard commercial and hermetic devices. Sequential HAST results for the LM124 devices indicate that the Dow Corning Ceramic Coatings do not degrade the electrical performance of the IC in assembly or burn-in.

Program Conclusions

Based on the work completed under this program, the following conclusions can be made:

1. Inorganic coated CMOS die in plastic packages surpasses the reliability of standard CMOS die by 600 hours to first failure in direct HAST exposure and approaches that of hermetic package reliability.

2. Weibull analysis of the plastic package reliability data reveals at least one order of magnitude decrease in failure rate was achieved through the use of protective inorganic coatings, applied prior to plastic encapsulation, as compared to standard plastic packages.

3. Low-temperature thin-film ceramic coatings do not degrade IC performance in assembly, burn-in, surface-mount assembly, or extended temperature cycling (-65 to 150°C), autoclave (121°C), and HAST (140°C, 159°C).

4. Device preconditioning, also referred to as sequential testing, accelerates the time to failure by 100 hours in HAST exposure of plastic packaged CMOS devices.

5. Reliability differentiation in HAST at 159°C was achieved between ceramic-coated and standard commercial die in plastic packages. Protection of ICs from moisture and mobile ions using thin-film ceramics increased device lifetimes in sequential HAST exposure by 300 hours over standard plastic encapsulated ICs.

6. Reliability differentiation in HAST at 140°C was not achieved on LM124 TapePaK™ and PDIP test devices through 1100 hours.

7, Reliability differentiation in autoclave, HAST, and temperature cycling/salt fog exposures was consistently achieved between ceramic-coated and standard die in ceramic, sidebrazed, unlidded chip carriers with aluminum wire.

8. Ceramic-coated aluminum leadwires, unprotected from mechanical shock and vibration, are susceptible to fracture at the bondwire neckdown to frame regions of the chip carriers.

Future Directions

This study establishes a comparative reliability database for standard commercial plastic encapsulated devices produced from state-of-the-art materials and processes at National Semiconductor. Significant improvement in device reliability was achieved by sealing the chip using Dow Corning's low-temperature ceramic coatings. The use of this technology at the wafer level is proposed. This will provide an economical packaging approach for supplying sealed chips to the semiconductor industry. This enabling technology will facilitate the development of known-good-die (KGD) for advanced packaging applications, such as multichip modules, by providing sealed devices which are reliable over extended long-term storage and service life.

BACKGROUND

Traditional plastic packaging has not been adequate for the rigorous demands of the military environment. Recent advances using state-of-the-art materials, processes, and package technologies have prompted new investigations to assess their reliability. This study evaluates the comparative effectiveness of plastic packaging with protective inorganic die coatings under extreme and differentiating temperature and humidity conditions. Additionally, comparative effectiveness of the reliability of bare die assembled in ceramic chip carriers were assessed for insertion into MCM applications.

Industry and government studies, throughout the development of integrated circuits and related processes, repeatedly have identified moisture and ionic contamination as major contributors to device failure. Step-wise improvements in the ionic impurity and adhesion of epoxy molding compounds (EMCs) have enhanced the reliability of plastic encapsulated devices. However, these materials have intrinsic high moisture permeability and absorptivity. Issues regarding the long-term storage and reliability of plastic packaged devices have not been adequately addressed. The high vapor permeability of EMCs permit water vapor and reactive ions to diffuse to the circuit elements, concentrate at interfaces, and corrode the circuit metallization. As shown in Figure 3, the permeability of epoxy (organic) materials is from three to seven orders of magnitude greater than that of glasses (inorganics) and metals [1].

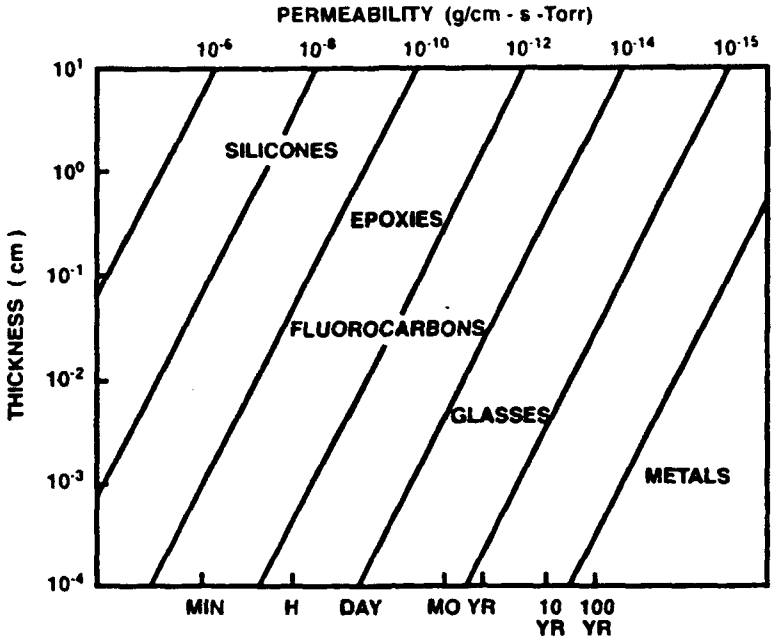


Figure 3. Moisture Permeability of Various Materials

Epoxy (organic) materials that are used for plastic packaging are permeable and can easily absorb moisture. In most cases, the plastic packages saturate with moisture quickly, as shown by the curves in Figure 4.

Current semiconductor trends to increase complexity, speed, circuit size, and to decrease geometries will exacerbate the intrinsic high moisture permeability of EMCs. Placing these circuits in hermetically sealed ceramic packages will provide adequate, long-term protection from these contaminants, but with increased size and weight tradeoffs. National Semiconductor Corporation and Dow Corning Corporation have independently pursued advance packaging technologies to enhance the reliability of plastic packaged ICs; an example of these technologies include TapePak™ and Low-temperature Inorganic Dielectrics respectively.

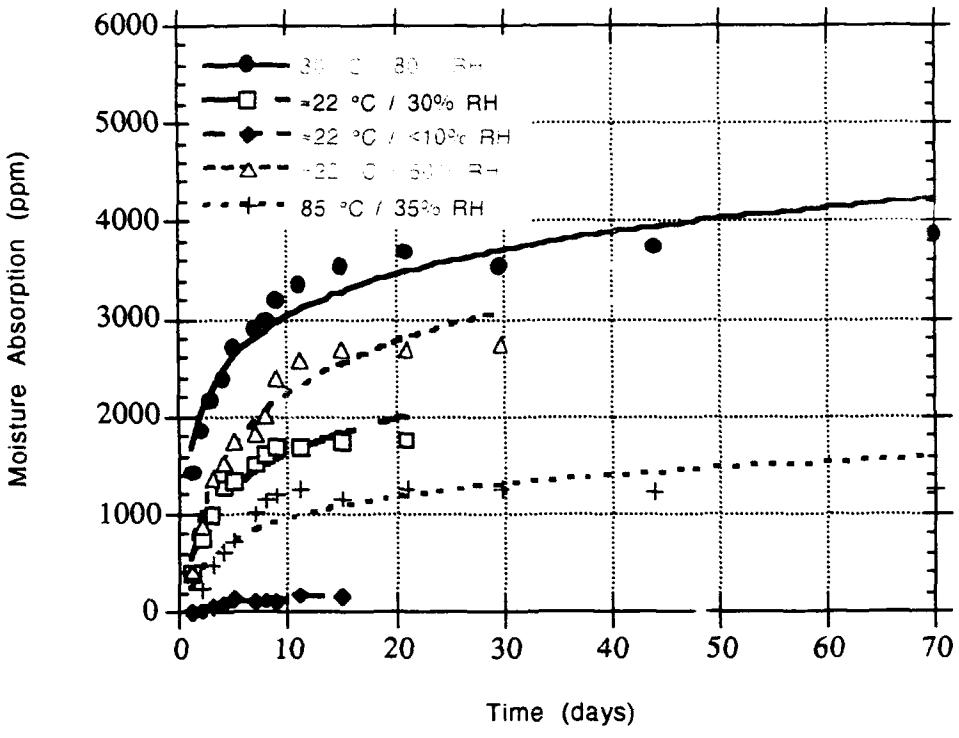


Figure 4. Moisture Absorption Profiles for 40-lead TapePak™ Under Various Ambient Conditions.

National Semiconductor TapePak™ Technology

National Semiconductor's TapePak™ technology is a low-cost, reliable, high-lead count capable package that can be less than 1/10 the size of a traditional dual in-line package (DIP) and 1/3 the size of other surface-mount devices such as a plastic leaded chip carrier (PLCC). TapePak™ uses tape-automated bonding (TAB) technology and a unique outer ring to protect the leads during shipping. The technology was designed to take full advantage of automatic assembly systems with their high speed and precision. It can be used with existing precision surface-mount assembly equipment with minimal modification. The only requirement is an accessory for removing the outer ring and forming the leads at the point of assembly.

TapePak™ also provides a significant improvement in the electrical characteristics of each package. Lead capacitance and inductance can be reduced up to ten times from that of other packages. Signal propagation time is also reduced and thermal characteristics improved. They survive stringent environmental tests such as autoclave at 121°C at 15 psig and temperature cycling from -65 to 150°C for 1000 cycles.

To further the technology in the industry and make these advantages available to everyone, National has registered TapePak™ specifications in JEDEC packaging committee as an industry standard. National has also licensed other manufacturers to use TapePak™ packaging for their own proprietary devices.

Dow Corning Low-temperature Inorganic Dielectric Coating Technology

Dow Corning developed a series of unique chemical precursors which can be applied as thin-films and converted to inorganic dielectrics at relatively low processing temperatures [2]. One of the applications for these advanced inorganic dielectric coatings include the environmental protection of ICs. The feasibility of using this new technology directly on silicon and gallium arsenide circuits was first studied under ARPA sponsorship [3]. This concept, originated by Dow Corning Corporation, was first known as the SPEC concept (Surface Protected Electronic Circuits) and integrated the use of two inorganic (ceramic) dielectric layers:

1. Silicon Dioxide Layer - for smoothing/planarizing the circuit topology, and
2. Silicon Carbide Layer - for a dense environmental barrier.

The feasibility study showed that the ceramic coatings clearly demonstrated protection of the circuits when exposed to autoclave, HAST (highly accelerated stress testing), and salt fog exposures without affecting the functions of the silicon or gallium arsenide test devices.

Several performance studies revealed that bare die protected by these low-temperature (<250°C) ceramic coatings withstood >500 hours of exposure to autoclave, HAST, salt fog and thermal cycling [4]. This two-layer coating system was further improved by adding a top layer of silicone gel for mechanical protection.

Air Force RWOH Program

This paper presents the results of a Wright Laboratory Manufacturing Technology (ManTech) program undertaken to assess the reliability of advanced packaging technologies using severe military environmental exposure. The mission of the Air Force RWOH program is:

> To evaluate the industry's most promising integrated circuit coating material for application in military systems. Testing and failure analysis data will be used to determine if non-hermetic integrated circuit packaging approaches appear feasible to replace standard hermetic packaging currently used in military systems. This program is to provide assessment data of integrated circuits in single chip packages. This data should establish the baseline technology directions for the eventual coating of multichip packages.

Specifically, this program will evaluate state-of-the-art plastic package reliability and an advanced inorganic (ceramic) protective coating system that will allow replacement of hermetic packages in commercial and military products. The goals of this contract effort are to establish baseline performance data on plastic packaged ICs, integrate the inorganic protective coatings into existing IC plastic packaging, and assess their performance through severe and differentiating environmental stress exposures. This concept is illustrated in Figure 5.

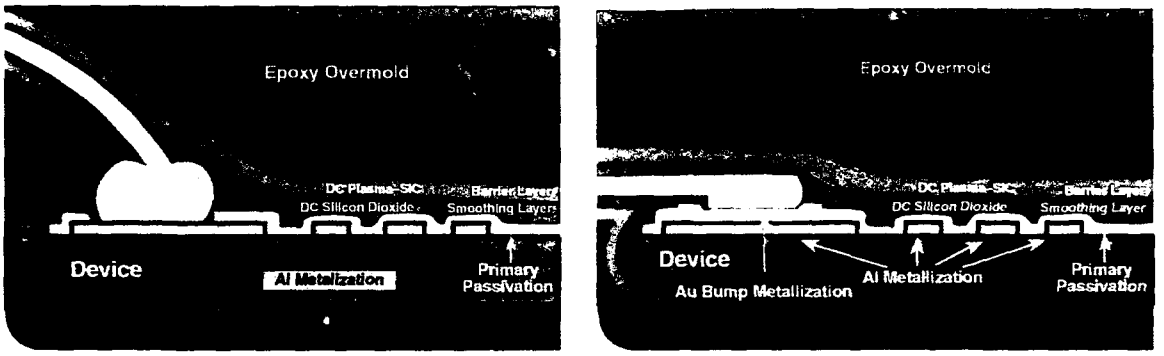


Figure 5. Ceramic/epoxy integrated circuit packaging structure for the NSC/DCC RWOH project.

Program Objective

The objective of this program is to assess whether integrated circuit reliability can be achieved without hermeticity using state-of-the-art packaging technologies. To achieve this objective, the following strategy was implemented:

1. Assess the reliability of commercial plastic packaged ICs.
2. Integrate low-temperature ceramic coatings into existing commercial plastic packaged ICs.
3. Assess the reliability of ceramic-coated plastic packaged ICs with respect to standard commercial ICs.
4. Assess the reliability of ceramic-coated bare die in chip carriers with respect to standard die for correlation with future multichip module (MCM) insertion.

Severe environmental stress tests were used to assess reliability. Comparative assessment will be made against standard die (no die coating) in traditional hermetic packages.

The role of the coating system is to protect the die surface and bonding pad areas by sealing the assembled device prior to plastic overmold. This study is the first attempt to integrate the ceramic coating technology into an existing plastic overmold process to produce a sealed chip with enhanced reliability. A high-volume CMOS and operational amplifer (linear) device were the test vehicles selected in this study.

SELECTION OF DEVICES; TEST VEHICLES

Selection Criteria

Various silicon integrated circuits were considered for this study which would most realistically assess the ceramic coating deposition processes, intrinsic material properties, and the moisture and ion protection providing enhanced device reliability. Criteria used for the selection of silicon integrated circuit devices for use as test vehicles in this study included:

1. The device is currently used by DoD;
2. The circuit behavior is well understood;
3. The circuit is readily available;
4. The circuit is sensitive to moisture;
5. The circuit is sensitive to ionic degradation;
6. The circuit lends itself to various packaging approaches.

Devices Selected: LM124 and CD4011B

For this study, the NSC LM124 operational amplifier (Op-Amp) and the NSC CD4011B CMOS integrated circuits were selected as the test vehicles.

The LM124 Low Power Quad Operational Amplifier consists of four independent, high-gain, internally frequency-compensated operational amplifiers which were designed to operate from a single power supply over a wide voltage range. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Four on-chip capacitors are sensitive to both mechanical stress and moisture ingress, which causes internal parametric shifts, and make this device ideal for this type of reliability testing. A complete data sheet, including both electrical and physical parameters for the LM124 is included in Appendix A.

The LM124 is normally packaged in the 14-lead DIP, both plastic and hermetic, and can be supplied as a plastic quad flat pack (PQFP), commercially known as TapePak™. When screened to Mil-Std-883, the hermetic device is sold to military customers. A picture of the LM124 TapePak™ is shown in Figure 6.

The NSC CD4011B CMOS Quad Dual Input NAND Gate is fabricated with P and N channel enhancement mode circuits in a single silicon monolithic structure. This logic device is very sensitive to ionic degradation which causes both functional and parametric shifts of field effect transistors (FETs) and input diodes, which make this device ideal for this type of reliability testing. A complete data sheet, including both electrical and physical parameters for the CD4011B is included in Appendix A.

The CD4011B is normally packaged in a 14-lead DIP, both plastic and hermetic. A picture of the CD4011B in a plastic package is shown in Figure 6. A picture of the CD4011B in a ceramic sidebrazed package is shown in Figure 7.

Both test vehicles/devices, LM124 and CD4011B, were assembled using best commercial practices. Except as noted herein, no special handling or processing was granted to the test devices in order to simulate, as close as possible, the real manufacturing conditions.

Assembly of Test Vehicles

A single wafer (wafer lot) was used for the assembly of both PDIP, hermetic, and cavity packaged CD4011B devices. A single wafer (wafer lot) was used for the assembly of the LM124 TapePak™ devices. These devices had a primary passivation consisting of plasma-SiN over plasma-SiO_2. A single wafer (wafer lot) was used for the assembly of the LM124 hermetic DIP controls and had a single plasma-SiO_2 layer passivation for better correlation with historical data on these devices. Typically, National uses a dual-layer passivation scheme with plasma-SiN over plasma SiO_2.

Assembly of 14-lead PDIP

The assembly of the 14-lead PDIP was performed in the Packaging Lab in National Semiconductor's South Portland, Maine facility. These parts were assembled with gold spot plated 14-lead PDIP leadframes, instead of the standard silver spot because of an incompatibility problem between the SiO_2 deposition process used prior to coating and the standard silver spot plating. Gold was used because of its excellent thermal, electrical, and noble properties. Drawings for the 14-lead PDIP leadframe are in Appendix B.

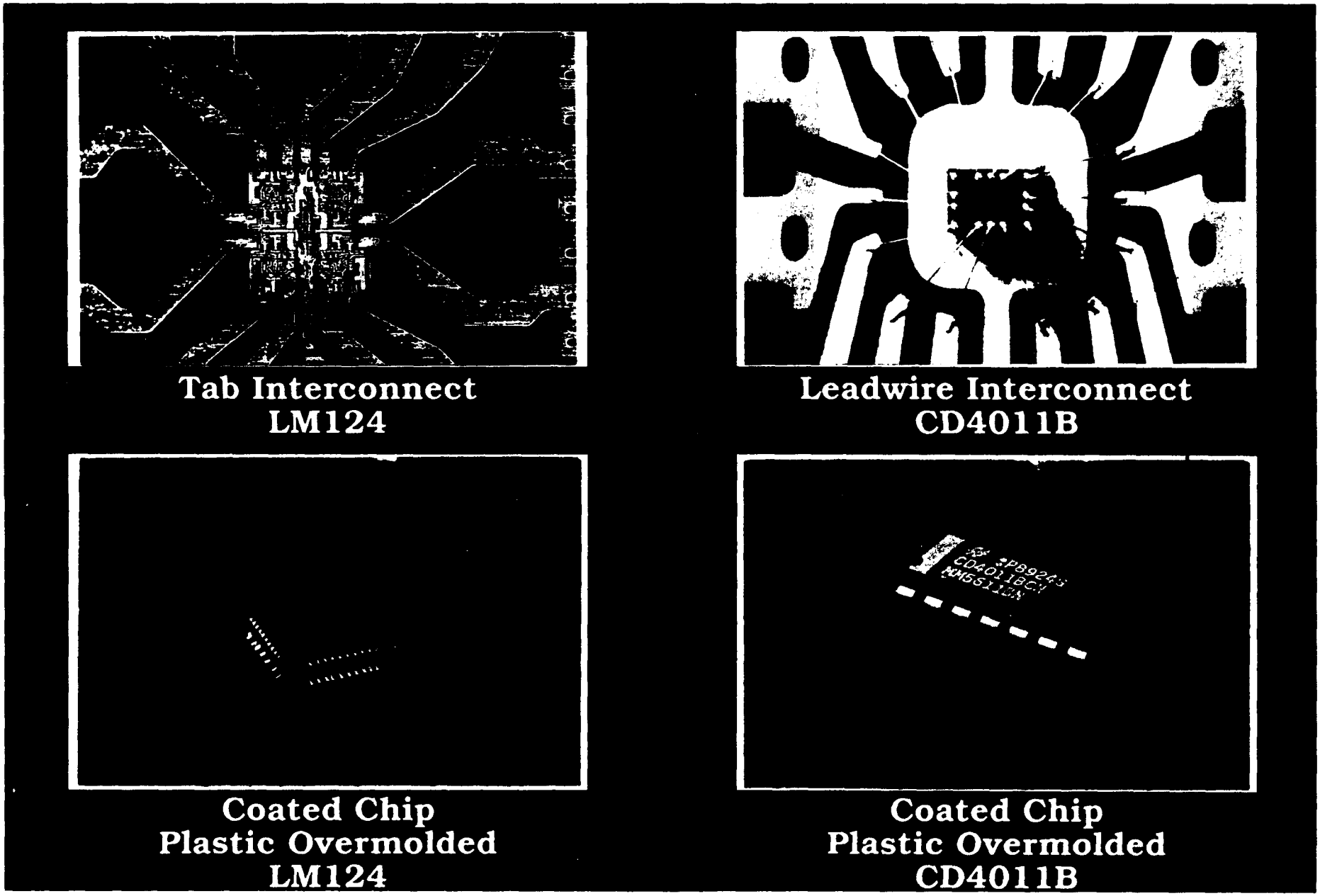


Figure 6. Pictures of the LM124 Op-Amp and CD4011B CMOS device before and after plastic packaging.

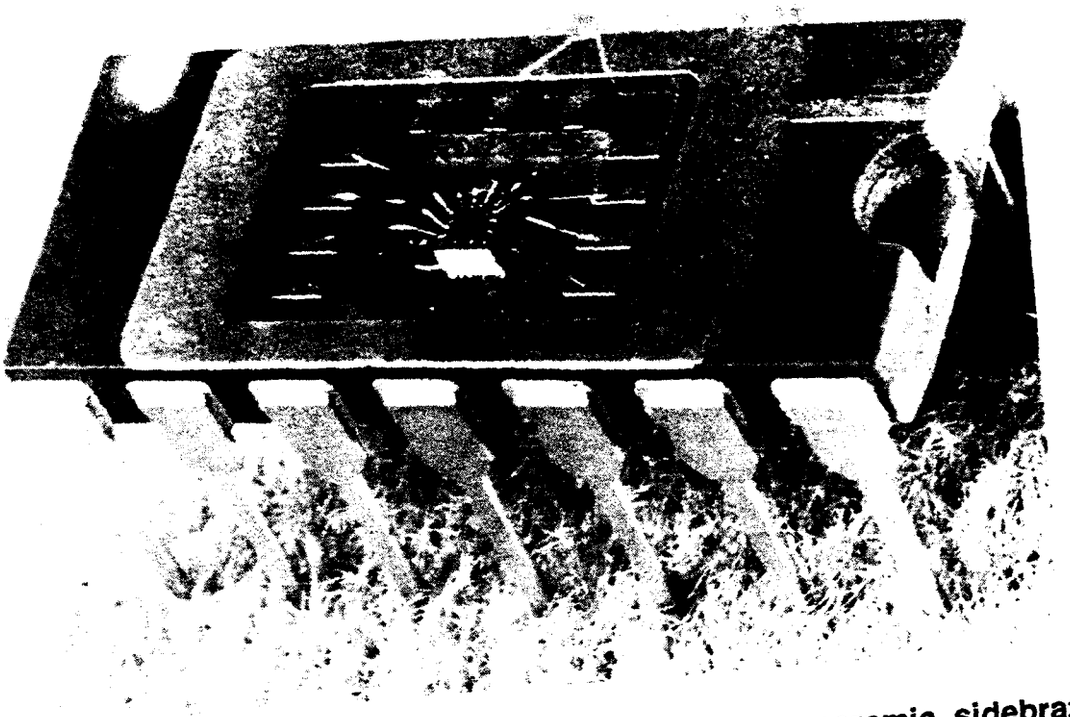


Figure 7. Picture of the CD4011B CMOS device in a ceramic sidebrazed package.

Both the CD4011B and the LM124 test vehicles were assembled in the 14-lead PDIP. The following is the process flow for the 14-lead PDIP:

1. 1st Optical Inspection
2. Wafer Saw
3. Polyimide Die Attach
4. Die Attach Cure
5. Inner Lead Bonding (Wirebond)
6. 3rd Optical Inspection
7. Epoxy Overmold
8. Mold Cure
9. Trim and Form
10. Solder Dip

In all cases, gold wire (99.99%) was used. 3rd Optical Inspection was performed to National's standard commercial practice.

Assembly of TapePak™ devices

Only the LM124 device was packaged in a 40-lead TapePak™ package. The assembly of the TapePak™ was performed by National Semiconductor's Singapore assembly facility in Southeast Asia. The nature of the technology used to assemble these devices is quite different that of the PDIP. TapePak™ utilizes tape automated bonding technology which requires a tri-level metallization of the device bond pads after deposition of the primary passivation. The lead bonding is performed in a single thermocompression bonding operation that bonds an etched copper leadframe to the metallized bond pad. The metallization system consists of an aluminum seed layer (4000Å), a nickel-vanadium barrier layer (3000Å), and a copper bonding layer (8000Å). This is deposited onto the bond pad by sputter deposition at low pressure. The pad is capped with a thin gold layer (400Å) via an immersion process for protection from corrosion. A schematic of the bond pad structure is shown in Figure 8. Drawings of the 40-lead TapePak™ leadframe can be found in Appendix B.

A single wafer (wafer lot) was used for the assembly of all LM124 TapePak™ devices which had a primary passivation consisting of plasma-SiN over plasma-SiO_2. The following is the TapePak™ assembly process flow:

1. 1st Optical Inspection
2. Wafer Saw
3. 2nd Optical Inspection
4. Inner Lead Bonding (TAB)
5. Epoxy Overmold
6. Deflash
7. Mold Cure
8. Dambar Removal and Deflash
9. Solder Plate
10. Mark

Assembly of 14-lead Sidebrazed DIP

The assembly of the ceramic 14-lead sidebrazed DIP was performed by the Mil/Aero Packaging Lab in National Semiconductor's South Portland, Maine facility. Both the CD4011B and the LM124 devices were packaged in hermetically sealed DIPs to be used as control devices. Additional CD4011B devices were assembled in the same package, but were not hermetically sealed (unlidded). The following is the production process flow used to assemble the 14-lead sidebrazed DIP:

1. Package Incoming Inspection
2. 1st Optical Wafer Inspection
3. Wafer Saw
4. 2nd Optical Wafer Inspection
5. Eutectic Die Attach
6. Inner Lead Bonding (Wirebond)
7. 3rd Optical Inspection
8. Solder Seal Package
9. 4th Optical Inspection
10. Mark
11. Fine/Gross Leak Testing

In all cases, aluminum wire (99% Al, 1% Si) was used. 3rd optical inspection was performed per Mil-Std-883, Method 2010, Class B.

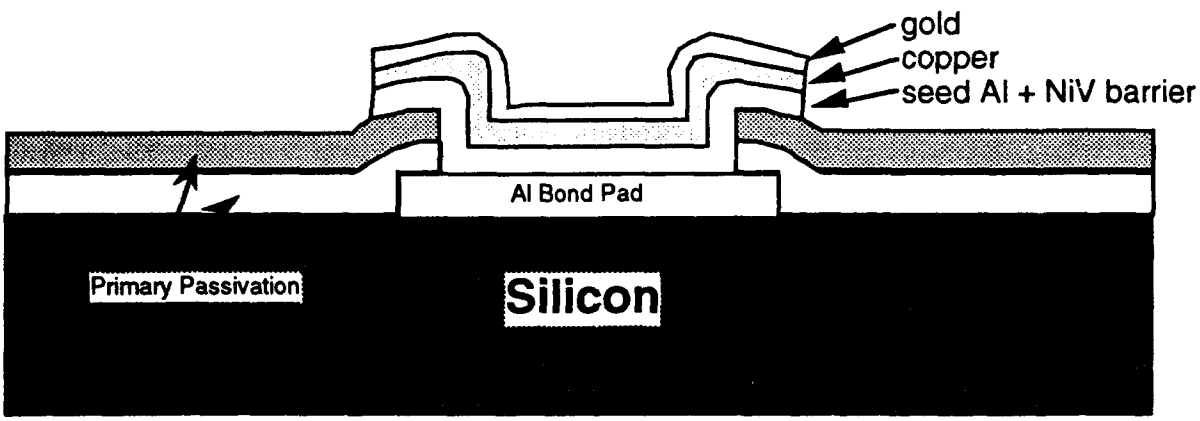


Figure 8. Schematic of Bond Pad Structure for LM124 40-Lead TapePak™ Device Showing Bond Pad Metallization (Al, NiV, Cu, Au).

EXPERIMENTAL

Application and characterization of the thin film ceramic coatings to partially assembled ICs mounted on leadframe and ceramic chip carriers was the primary focus of the experimental effort. This effort included process development, mechanical and electrical characterization, and engineering studies (adhesion) of the solution applied silicon dioxide layer and the vapor deposited silicon carbide layer. Throughout the coating process development, several environmental exposures were performed to assess a variety of process conditions including surface preparation, chemical precursors for SiO_2 and plasma-SiC, application techniques, precursor conversion, and deposition processes. Ceramic-coated CMOS devices processed at 250°C consistently achieved and reproduced circuit protection for over 300 hours of autoclave and HAST exposures regardless of surface preparation, application / deposition process, precursor conversion method.

Surface Preparation for Coating

Application of submicron thin-film ceramic coatings consisting of silicon dioxide and amorphous hydrogenated silicon carbide to integrated circuits mounted to chip carriers posed several key technical challenges. Consideration to the IC assembly process, materials of construction, and handling/shipping of these partially packaged devices was made to assure the highest possible coating integrity without altering National's standard production processes.

The assembly of the IC die in DIPs was completed in National Semiconductor's South Portland, Maine Packaging Laboratory using standard materials and processes. This work was not done in a cleanroom environment. Particle or organic surface contamination from wafer sawing, die attach/wire bonding processes, and equipment are not considered to be a problem since the existing primary passivation should protect the IC die during the packaging process. However, subsequent application of ultra thin-film, submicron coatings to these surfaces without complete removal of these process contaminants may result in substantial coating defects, voids, or loss of adhesion.

Effective sealing of the circuit substrate and I/O interconnect (wirebond or TAB) by the ceramic coatings requires adequate adhesion of the silicon dioxide coating to various materials. Materials used in the assembly of integrated circuits include gold, silver, copper, nickel, aluminum, silicon, and plasma-SiN films. These assembly

materials were incorporated into the surface preparation/cleaning study to assess the adhesion of the solution applied silicon dioxide layer derived at both 175 and 250°C. Polished silicon wafers were initially used as test substrates with metal films deposited by sputtering and the plasma-SiN films deposited by PECVD. Later, actual test devices were used as test substrates .

Cleaning Techniques

Various cleaning techniques typically used in semiconductor and hybrid assembly applications were used to assess their effectiveness in removing organic and particulate surface contaminants. Cleaning techniques used in this study included ultraviolet (UV)/ozone, soft plasma (using argon and oxygen, either individually or sequentially, at both 50 and 200 W), and solvent vapor degreasing. These cleaning techniques were initially assessed using surface analytical techniques and later compared for differences in adhesion properties of the silicon dioxide film.

Both UV/ozone and soft plasma cleaning provided effective removal of organic contaminants but did not reduce surface particles. The soft plasma technique in all cases re-contaminated the surface with fluorinated hydrocarbons originating from teflon fixtures within the plasma unit. There were no available ceramic replacement parts. Isopropyl alcohol (IPA) vapor did remove a majority of visible surface particles but was not effective in removing organic contaminants. Furthermore, the IPA vapor deposited hydrocarbon and alcohol residues on the surface. Figure 9 shows IR spectra of residual contamination from soft plasma and IPA vapor cleaning techniques. Figure 10 shows X-ray photoelectron spectroscopy (XPS) of an aluminum substrate before and after soft plasma cleaning identifying a fluorinated hydrocarbon contaminant.

A sequential cleaning process incorporating first an IPA vapor followed by UV/ozone was effective in removing both particulate and organic contamination from test substrates and actual IC die.

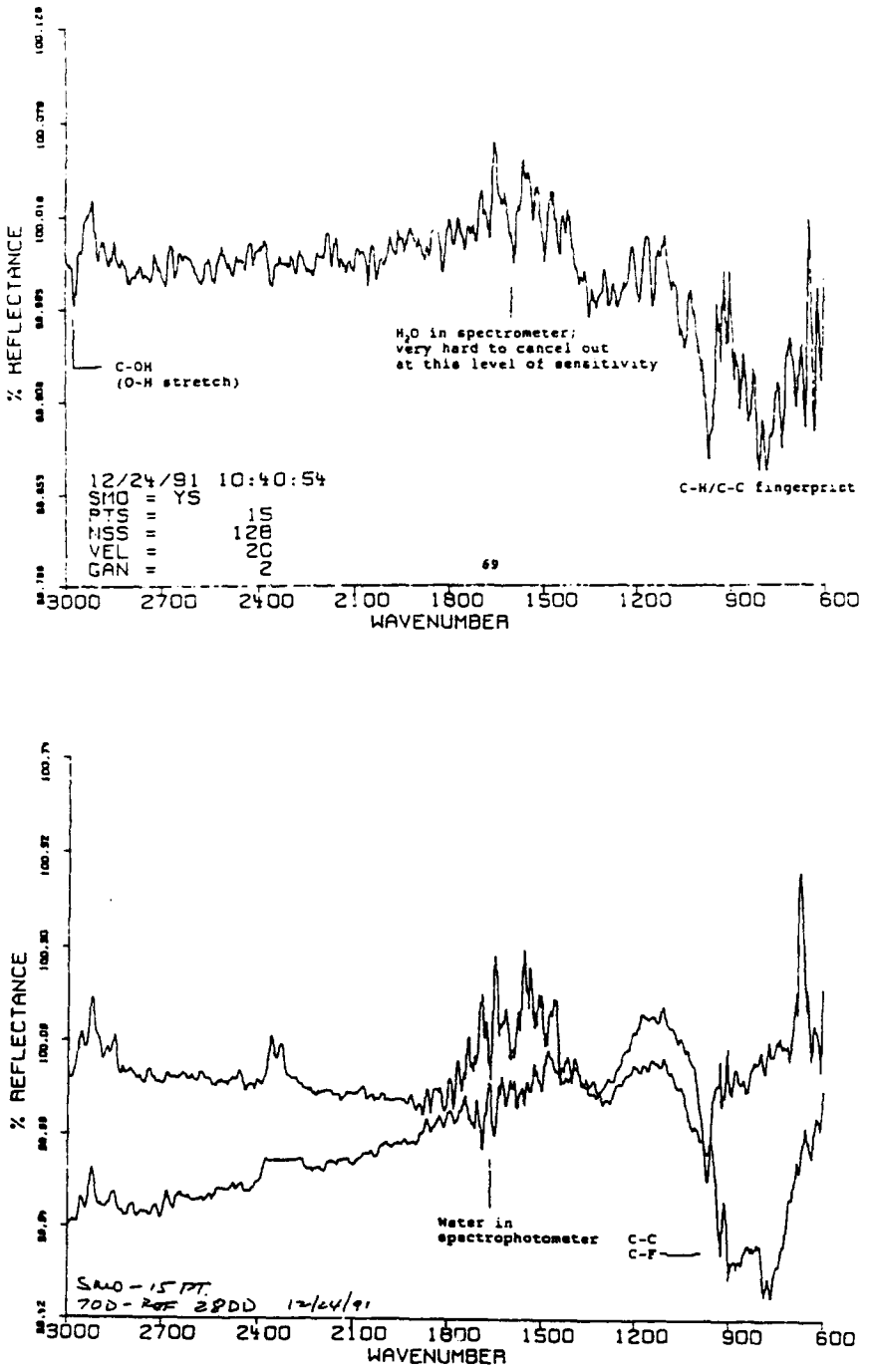


Figure 9. IR Spectra of a substrate cleaned by IPA vapor (top) showing hydrocarbon residue and soft plasma (bottom) showing fluorinated hydrocarbon residues.

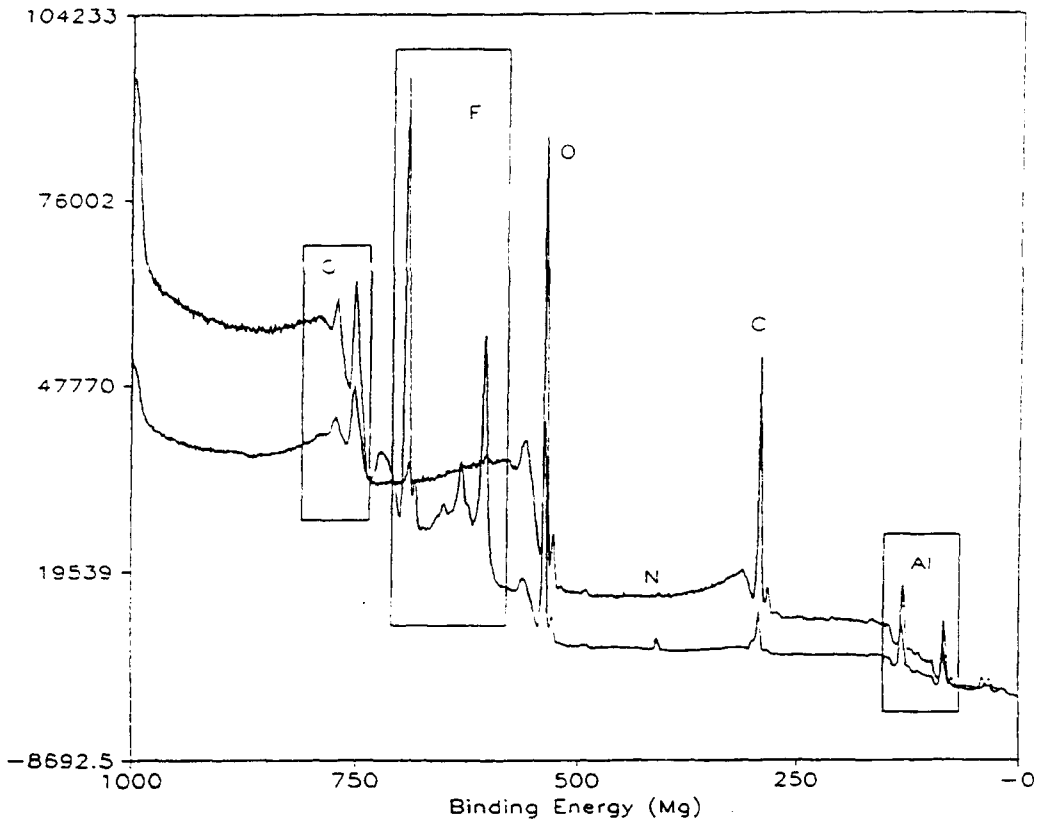


Figure 10. XPS Spectra comparing an aluminum substrate before and after soft plasma cleaning identifying a fluorinated hydrocarbon contaminant.

Adhesion Methodology

The metal films (materials) pose a variety of problems for selecting an appropriate adhesion test method for thin films due to the inherent low modulus and ductility of these metals as well as the diversity of coefficients of thermal expansion and reactivity. No problems were expected in testing the adhesion of the silicon dioxide film on the plasma-SiN passivation.

Most of the adhesion test data reported in the literature for ultra thin-films were obtained through two different types of stresses generated at the interface between the film and the substrate: tensile and shear tests [5]. Several adhesion test methods were considered for this study as a result of an exhaustive literature search, although not much activity has been documented for films <1.0 μm in thickness. Therefore, an

attempt was made to characterize the adhesion of the silicon dioxide film by several techniques. Four adhesion test methods were chosen as candidates for measuring the practical adhesion of the thin-film, based on the stress typically encountered in service as well as the reproducible nature of the test method:

Stud Pull Test	Tensile force
Scratch Test	Shear force
Cross Section	Tensile and shear forces
Tape Test	Shear and peel forces

The stud pull adhesion test has been accepted as an industrial standard since it is a direct measure of a thin film's intrinsic mechanical characteristics. This is an easily performed quantitative test with well known limitations and strengths. The scratch adhesion test is gaining momentum in the assessment of well adherent engineering thin films [5]. The information currently available on this new technique indicates it is a very versatile test, is easy to perform, and is a comparative measure of adhesion (critical load, L_C) [5].

The results of an initial feasibility study revealed that the tape-pull test was the only test method yielding consistent data for assessing the adhesion of the ultra thin-film silicon dioxide coating on metal sputtered silicon wafer substrates.

Adhesion Characterization Results

The coating adhesion was assessed by tape-pull tests using three peel strengths of tape, the highest being 78.2 oz/in width, followed by optical or SEM examination. There were no significant differences on the adhesion of silicon dioxide films between the UV/ozone and the soft plasma cleaning processes. The silicon dioxide films had strong adhesion to aluminum, silicon, nickel, and plasma-SiN films regardless of the cleaning method or conversion temperature. Moderate adhesion was obtained on copper and gold and low adhesion to silver. Subsequent exposure to 100 temperature cycles at -65 to 150°C or 100 hours of autoclave at 121°C, 100% RH also did not differentiate between cleaning processes. The adhesion of the hydrogen silsesquioxane derived silicon dioxide coating was consistently improved when those coated test substrates were exposed to temperature cycling. Difficulty in cleaning silver was experienced by both UV/ozone and plasma methods due to extensive oxidation of silver leading to a very loose and powdery silver oxide or silver

peroxide. This accounted for the low adhesion of silicon dioxide to silver.

Silicon Dioxide Smoothing Layer

Chemical Precursors for Silicon Dioxide

Hydrogen silsesquioxane, $(HSiO_{3/2})_n$, was the primary candidate chemical precursor for the silicon dioxide layer. Four alternate precursors and the properties of the resulting silicon dioxide films were investigated by directly substituting these alternate precursors for hydrogen silsesquioxane in the coating process. Some of these alternate precursors contained carbon in addition to silicon, oxygen, and hydrogen to provide some variation in mechanical properties which could enhance the maximum crack-free qualities of the silicon dioxide coating in thick cross-sections. The candidate precursors included polysilicate and polysiloxane chemistry which were repeatedly synthesized and characterized. The basic chemical structures of these candidate precursors are shown in Figure 11.

The solution-applied polysilicate and polysiloxane precursors to derive silicon dioxide have been traditionally used at high temperatures (≥400°C) as interlayer dielectrics. For use as a smoothing layer in device protection, conversion of these precursors to ceramics at temperatures <250°C is required to limit/reduce Kirkendall voiding. The film properties of the silicon dioxide layer produced from these alternate chemical precursors at low temperatures were inferior to those derived from hydrogen silsesquioxane.

Preliminary studies with alternate chemical precursors containing colloidal silica did reveal a greater resistance to cracking. Further studies revealed that the addition of colloidal silica hindered the vital smoothing characteristic of the chemical precursor reducing the cross-sectional thickness at the inner lead (ILB) and outer lead bond (OLB) regions. Consistent crack-free coatings at the bond pad regions were not achieved when these modified precursors were directly substituted into the coating process and therefore would not be used in any subsequent coating effort.

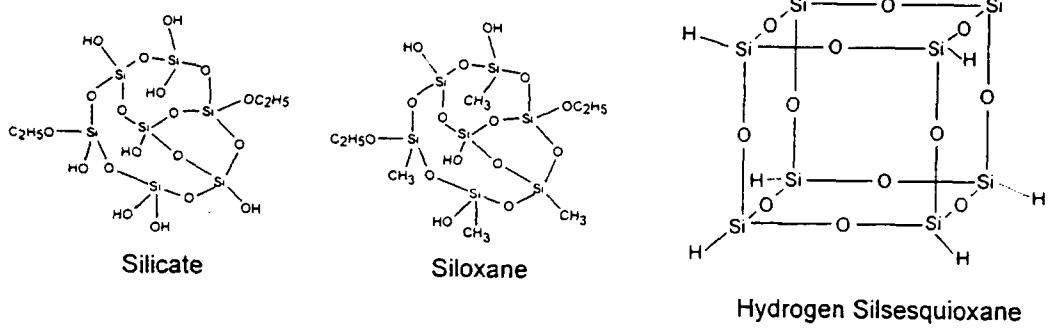


Figure 11. Chemical Structures of Candidate Silicon Dioxide Precursors

Hydrogen silsesquioxane was shown to be generally superior as the chemical precursor for the low-temperature silicon dioxide layer. This superiority was ultimately demonstrated by two series of parallel exposures of dual-layer coated CMOS circuits in extended autoclave and HAST environmental stress conditions. In both cases, only those circuits coated with hydrogen silsesquioxane derived silicon dioxide prior to plasma-SiC provided adequate surface protection. Characterizations of hydrogen silsesquioxane derived silicon dioxide coatings at 250°C provided a basis for understanding the circuit protection that was obtained. Hydrogen silsesquioxane produced the best coating characteristics, with greater circuit coverage and smoothing, as shown in Figures 12 and 13, and to yield a silicon dioxide layer with the least pinholes, the greatest film density, 2.03 g/cm^3, adequate permittivity (dielectric) properties, dielectric constant of 4.3 - 4.8 and loss factor of <0.06 at 11.1 GHz.

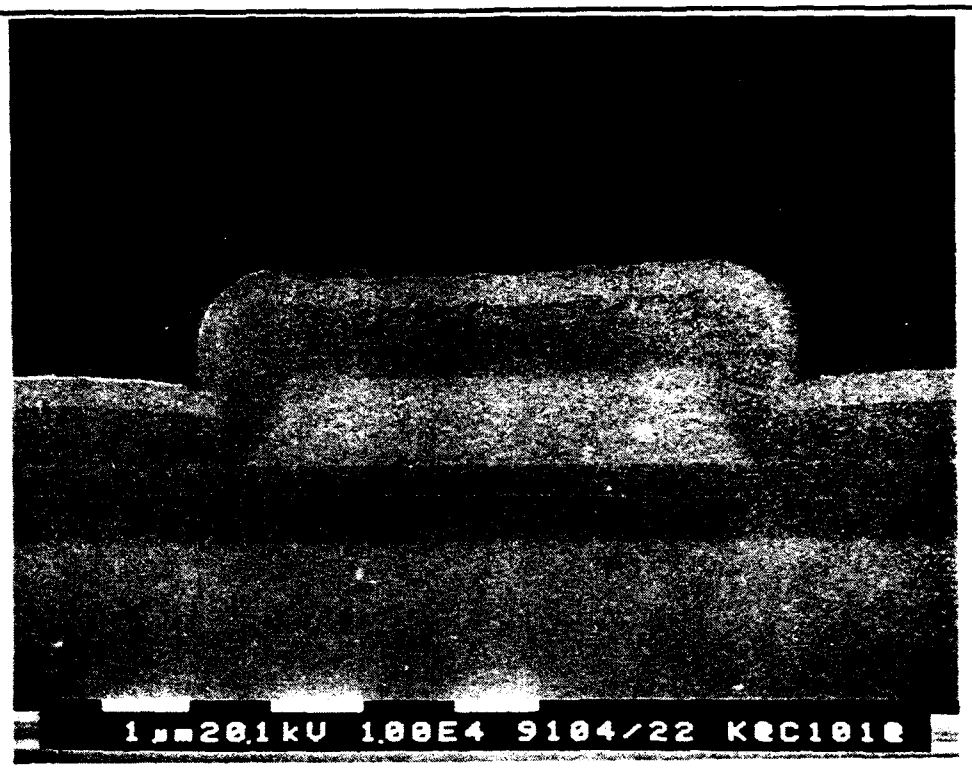


Figure 12. SEM cross-section of the center region of an IC after application of the silicon dioxide layer.

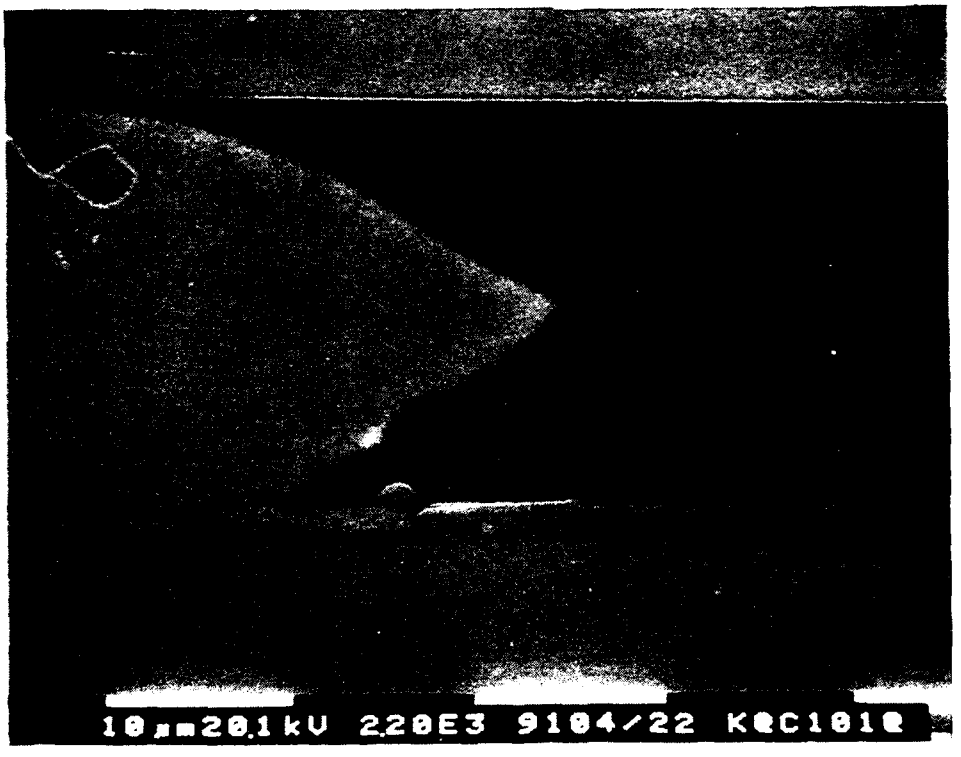


Figure 13. SEM cross-section of the bondpad region after application of the silicon dioxide layer.

Synthesis of Hydrogen Silsesquioxane

Hydrogen silsesquioxane is synthesized using a scarce water hydrolysis of trichlorosilane in a toluene/SO_3 fortified sulfuric acid reaction medium [6]. This process is followed by an extensive work-up of the organic layer to remove the residual acid and then the hydrogen silsesquioxane is isolated in solid form:

$$CH_3C_6H_5 + H_2SO_4/SO_3 \longrightarrow CH_3C_6H_5SO_3H + H_2O \quad (1)$$

$$n[HSiCl_3] + 3/2\ n[H_2O] \longrightarrow (HSiO_{3/2})_n + 3n[HCl] \quad (2)$$

In summary:

$$HSiCl_3 \xrightarrow[\text{Toluene}]{H_2SO_4/SO_3} (HSiO_{3/2}) + 3\ HCl \quad (3)$$

Followed by purification/isolation.

Typical Properties of Hydrogen Silsesquioxane

Typical physical properties of hydrogen silsesquioxane are listed in Table 1 [7].

Table 1. General Properties of Hydrogen Silsesquioxane

White Solid
Softens and flows at 180°C
Low concentration of ions, <10 ppb
Soluble and stable in hydrocarbon solvents
Coating application: by spin, spray, dip or flow
Converts at low temperature to chemically pure silicon dioxide

Conversion of Chemical Precursor to Silicon Dioxide

The hydrogen silsesquioxane can be converted to silicon dioxide by exposure to a variety of reaction conditions at low temperatures. Most low temperature conversions, 175°C and 250°C, may be performed in an aqueous ammonia environment within a few hours. Plasma oxidation of the chemical precursor was explored as an alternate process for converting the precursor to silicon dioxide. Prior experience at Dow Corning had shown that an oxygen plasma process at 250°C completely converts hydrogen silsesquioxane. Although both the ammonia and plasma conversion processes were shown to convert the precursor to silicon dioxide,

the size of the leadframe chip carrier approached the maximum substrate dimension for the PECVD chamber and limited the throughput for coating statistical quantities of devices for this study. Consequently, all further conversions of hydrogen silsesquioxane layers at 175 or 250°C were performed using aqueous ammonia in a tube furnace. This permitted a batch process of 80 coated leadframe strips (two magazine carriers) to be converted in a single process run. FTIR analyses shown in Figures 14 and 15 revealed that hydrogen silsesquioxane was completely converted to silicon dioxide at 250°C as indicated by the complete removal of SiH moieties at 2260 cm^{-1}.

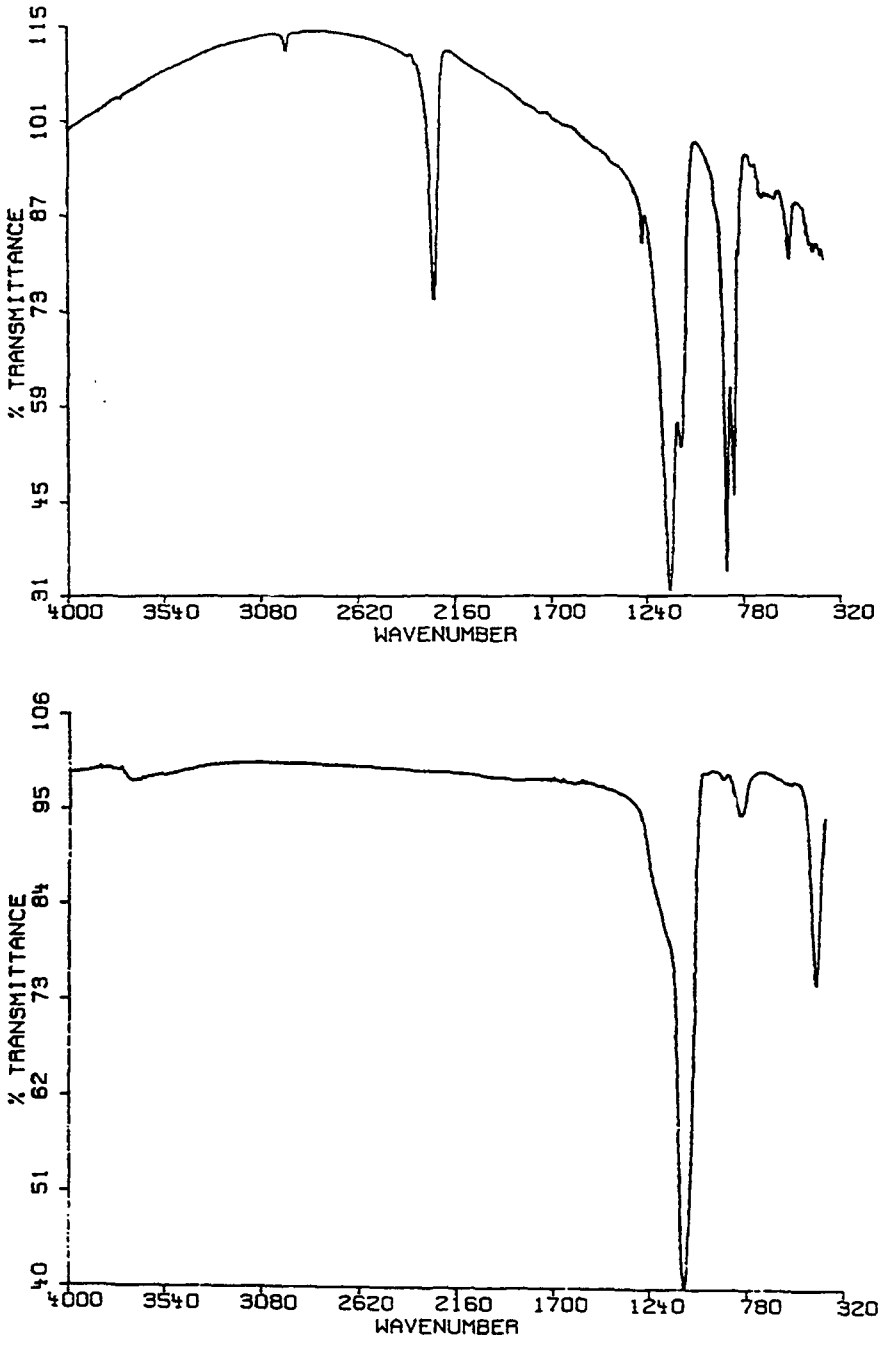


Figure 14. FTIR spectra illustrating the conversion of hydrogen silsesquioxane (top) to silicon dioxide (bottom).

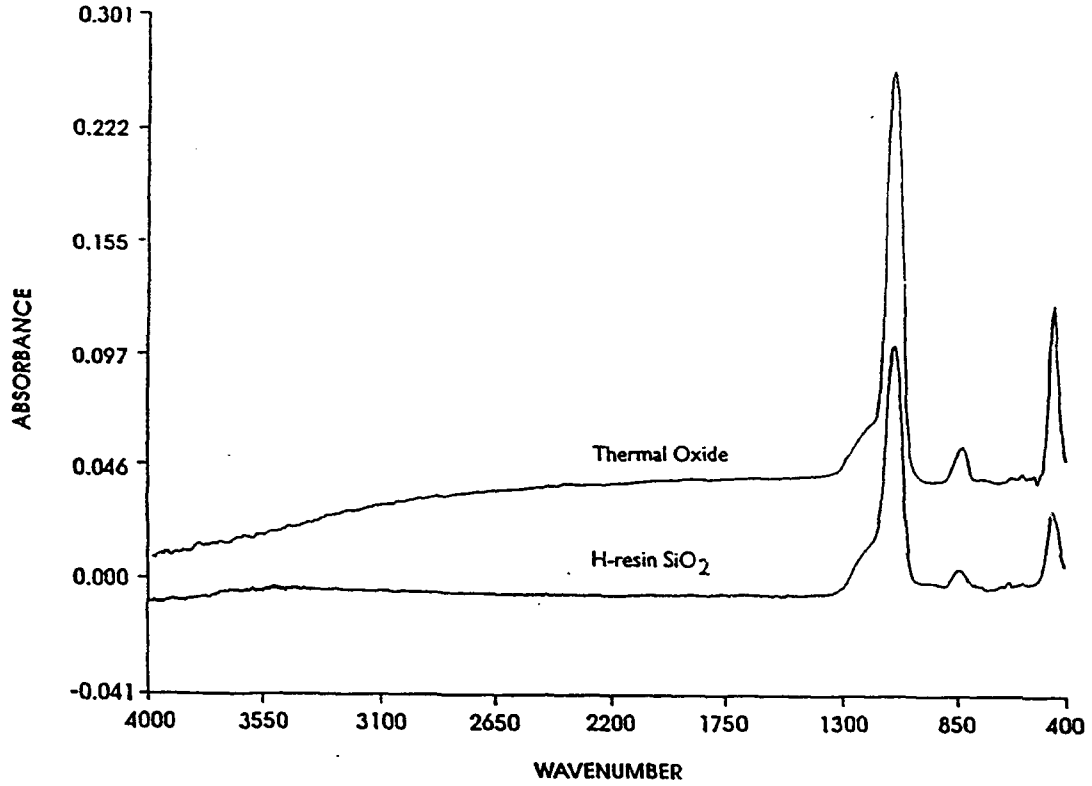


Figure 15. FTIR spectra comparing a silicon dioxide film derived from hydrogen silsesquioxane to a thermal oxide.

Characterization of Silicon Dioxide Layer

The mechanical and electrical properties of the hydrogen silsesquioxane derived silicon dioxide coating at 250°C are summarized in Table 2.

Table 2. Characteristics of Silicon Dioxide Processed at 250°C

Mechanical		
	Stress (MPa)	100-200 (T)
	CTE (ppm/°C)	1.5
	Adhesion:	High - Al, Ni, and Si, and Plasma-SiN
		Moderate - Cu and Au
		Low - Ag
Electrical		
	Dielectric Constant	3.8-4.8
	Loss Factor	<0.06
	Volume Resistivity (ohm-cm)	$>10^{11}$
	Dielectric Strength (V/μm)	>75
Microstructural/Morphological		
	Composition: (X:Si)	1.9-2
	Pinholes (Glassivation Test)	Pass
	Density (g/cm^3)	1.7-1.9

Ultrasonic Spray Application of Chemical Precursor

Ultrasonic spray coating proved to be the preferred method for applying the chemical precursor to chip-on-tape and leadframe chip carriers, particularly when areas must be masked. This application method atomized the hydrogen silsesquioxane solution into 10-20 μm particles, producing a fog which was found to provide high solution penetration on these non-planar surfaces. The solution formulation, flow rate, device temperature, transport speed, and distance from the nozzle to the device were varied to determine the optimum spray conditions. Figure 16 shows the basic equipment used for ultrasonic spray application and, in greater detail, the spray nozzle above the parts to be coated.

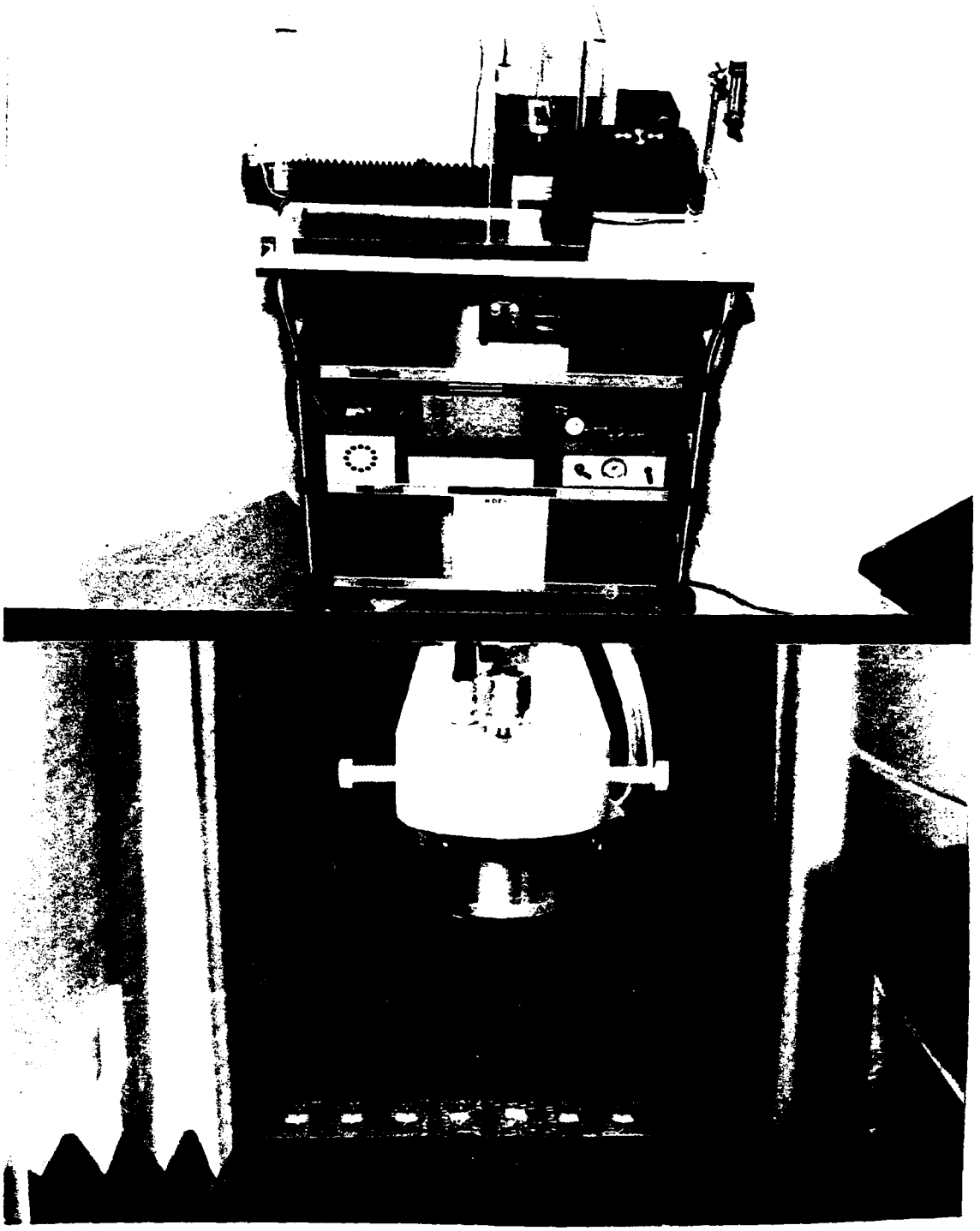
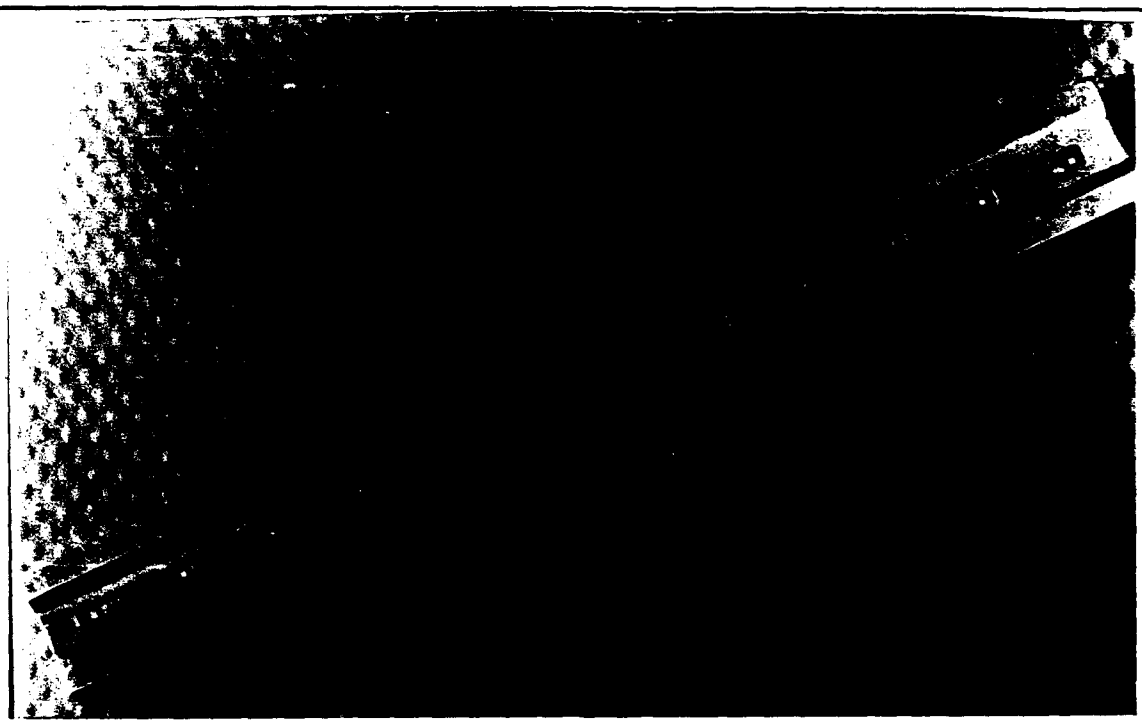


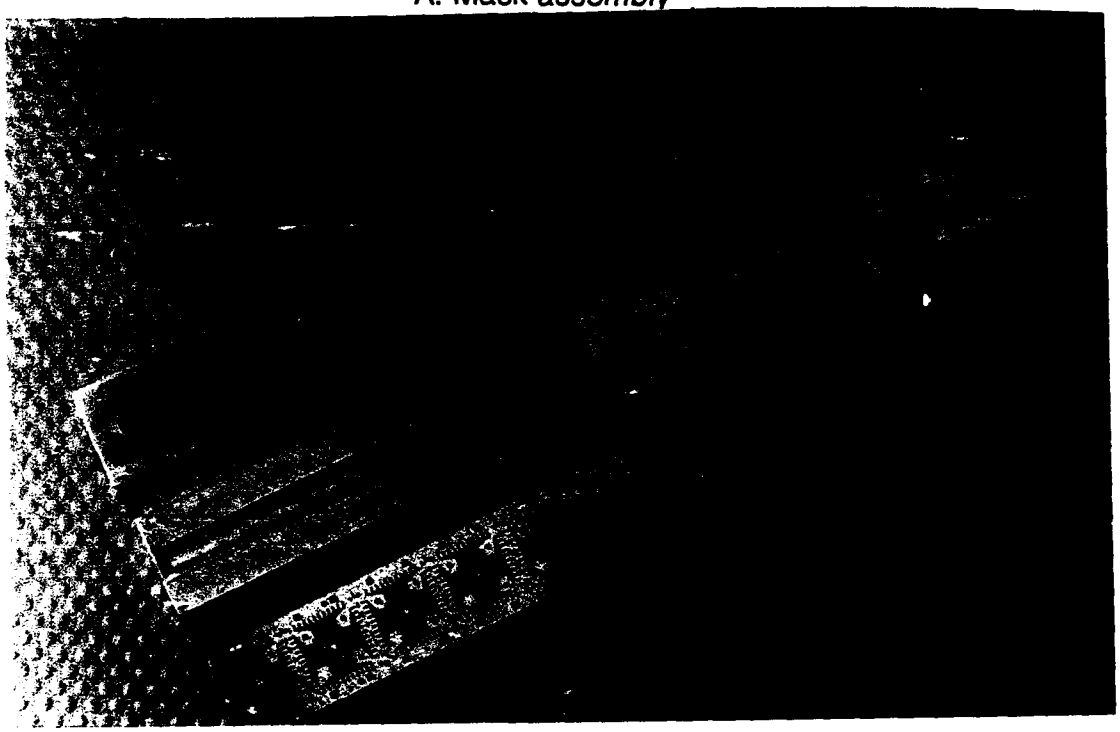
Figure 16. Ultrasonic spray system.

Spray Coating with a Mask

A stainless steel shadow mask was fabricated to confine the spray coating to only the die and interconnect regions of TAB and wire bonded circuits. Figure 17 shows the mask assembly for LM124 leadframes and Figure 18 shows the mask assembly for CD4011B leadframes.

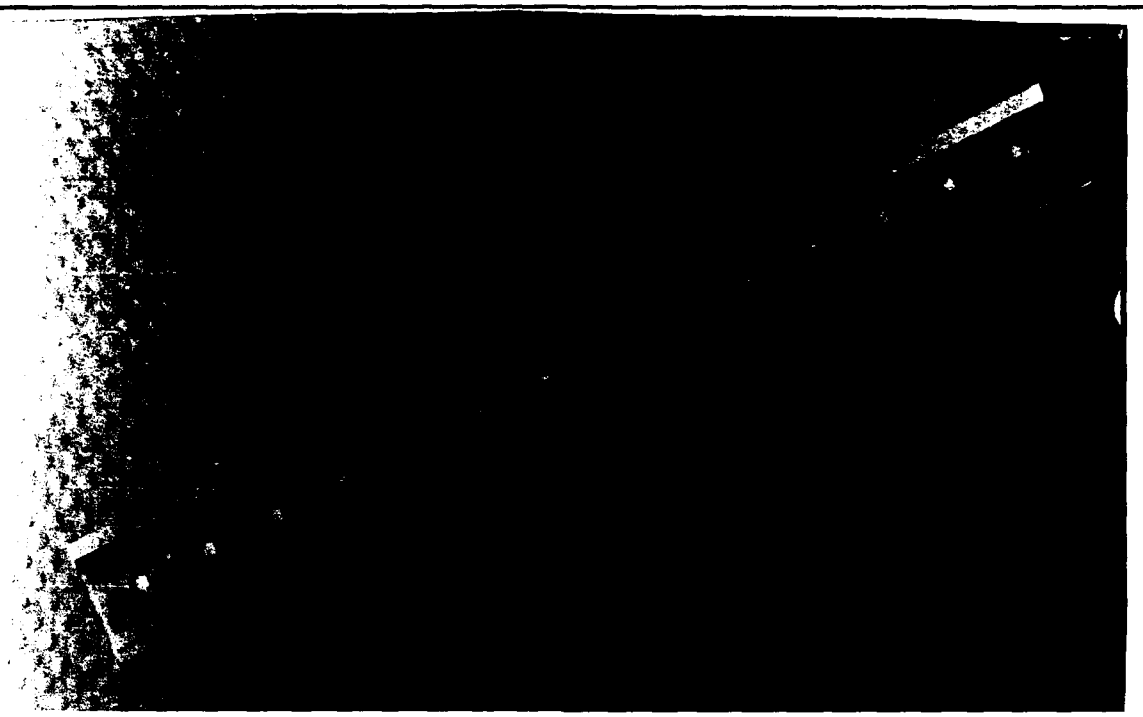


A. Mask assembly

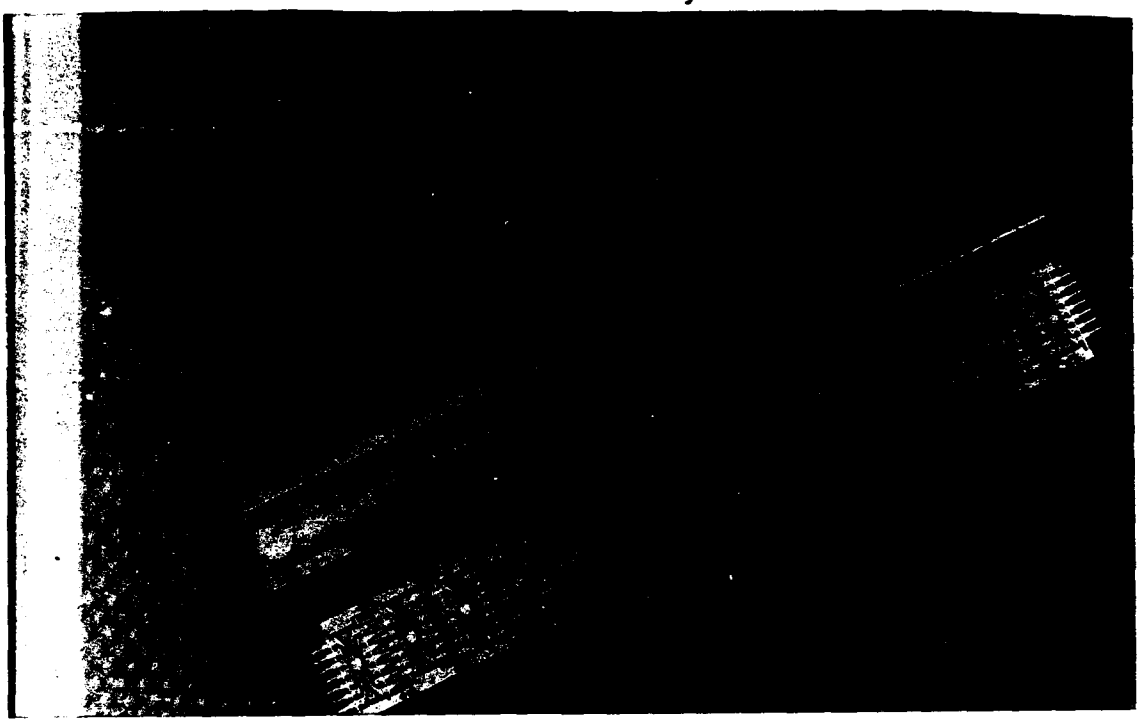


B. Mask disassembled

Figure 17. Spray coating mask for LM124 leadframes.



A. Mask assembly



B. Mask disassembled

Figure 18. Spray coating mask for CD4011B leadframes.

Assessment of Spray Coating

Assessment of the silicon dioxide coating coverage afforded by ultrasonic spray application was performed by SEM after intentionally damaging the device for coating identification. Figure 19 shows the typical coverage on a leadwire. Figure 20 shows the cross section of a coating on the edge of a die. Figure 21 shows typical coverage on a beam of a TapePak™ leadframe.

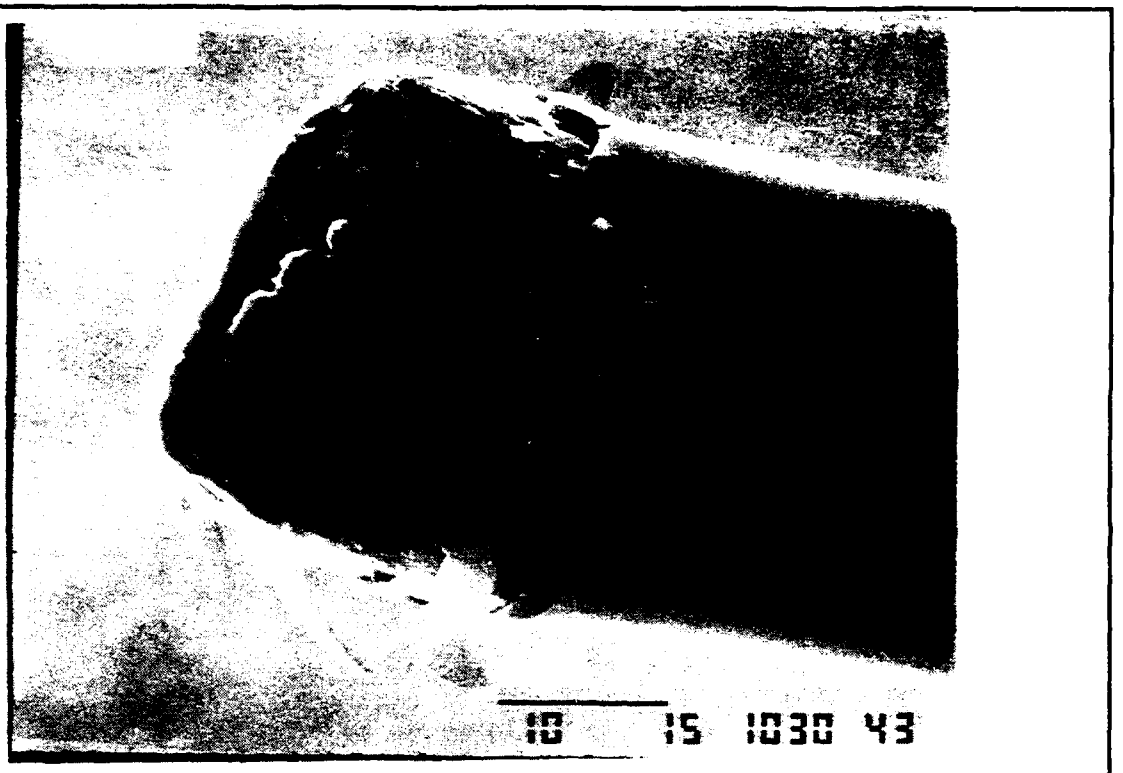


Figure 19. Coverage of silicon dioxide, applied by ultrasonic spray, on a leadwire from a CMOS device.

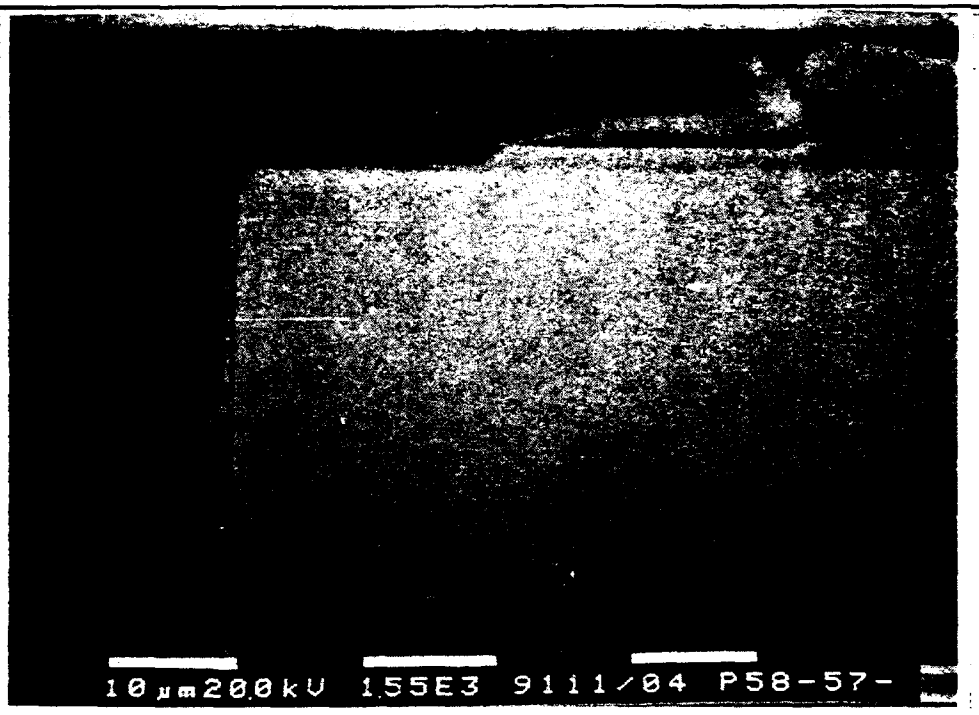


Figure 20. Coverage of silicon dioxide, applied by ultrasonic spray, on the side of CMOS chip.

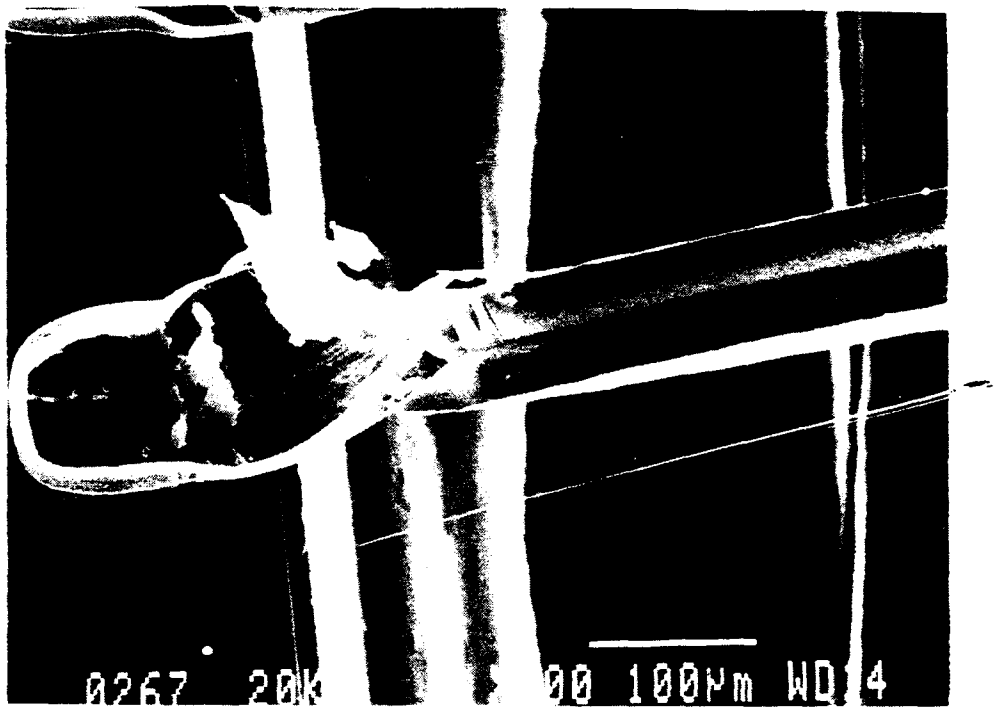


Figure 21. Coverage of silicon dioxide, applied by ultrasonic spray, on beam of TapePak™.

Amorphous Hydrogenated Silicon Carbide (a-SiC:H) Barrier Layer

The barrier layer provides the primary protection of the ceramic-coated integrated circuit from harsh environmental stresses. The silicon dioxide layer smoothes the circuit surface to minimize mechanical and electrical stresses in the barrier layer and isolates the circuit surface. The silicon carbide barrier layer, deposited by plasma-enhanced chemical vapor deposition (PECVD), is regarded in the scientific community as an amorphous hydrogenated silicon carbide (a-SiC:H) film; also referred to as plasma-SiC. Prior studies, performed under Dow Corning funding or prior DoD sponsorship, showed that deposited plasma-SiC layers provide exceptional protection as a barrier layer and can be deposited at practical rates with high reproducibility [7,10,11,15]. For this project, the prior studies were extended to include an alternate precursor material, refinement of process factors and control, development of masks, and procedures for depositing through masks.

Chemical Precursors for Plasma-SiC

Based on prior studies, silacyclobutane (SCB) was chosen as the primary chemical precursor for the plasma-SiC barrier layer [8]. Recently the use of methylsilane to deposit plasma-SiC films by PECVD has been reported [9]. This alternate precursor and the properties of the resulting plasma-SiC films were vestigated by directly substituting methylsilane for silacyclobutane in the current plasma-SiC process.

Typically, the deposition rate using methylsilane was lower than that observed with SCB. The behavior of the deposition rate with carrier gas was the same, increasing when argon is used. Keeping all of the deposition parameters constant, the substitution of methylsilane produced plasma-SiC film with a number of differences when compared to the standard silacyclobutane process; films deposited from methylsilane exhibited higher stress and refractive index. Comparison of infrared spectra show that the films deposited from methylsilane have a lower carbon concentration and most of this carbon is bound as CH_3 entities, whereas an amorphous, carbon-rich, bonding network is observed for films deposited from SCB. This result correlates with the lower amount of carbon in the methylsilane precursor.

Environmental testing of a limited quantity of ceramic-coated CMOS devices using methylsilane for the a-SiC:H precursor showed marginal improvement in device

reliabilty when compared to a control group of uncoated devices and performed poorly when compared to those coated with SCB derived a-SiC:H. While these results do not suggest that good protective plasma-SiC coatings cannot be produced from methylsilane, it is obvious that this precursor cannot be directly substituted into the established process for silacyclobutane. Based on these initial comparisons, SCB was used to produce the plasma-SiC coatings.

Synthesis of Silacyclobutane

Silacyclobutane is synthesized in three steps: $HSiCl_3$ addition to an allyl halide, cyclization, and reduction to silacyclobutane [10]:

$$HSiCl_3 + CH_2{=}CHCH_2Cl \xrightarrow{Pt} Cl_3SiCH_2CH_2CH_2Cl$$

$$Cl_3SiCH_2CH_2CH_2Cl \xrightarrow[-MgCl_2]{Mg/solvent} Cl_2Si\begin{matrix}CH_2\\ \\ CH_2\end{matrix}CH_2$$

$$Cl_2Si\begin{matrix}CH_2\\ \\ CH_2\end{matrix}CH_2 \xrightarrow[Metal\ chloride]{Metal\ hydride} H_2Si\begin{matrix}CH_2\\ \\ CH_2\end{matrix}CH_2$$

Silacyclobutane is a colorless liquid which boils at 42°C. It has been fully characterized by gas chromatography (GC), mass spectrometry, and nuclear magnetic resonance (NMR) [11].

Decomposition of Silacyclobutane

Thermal or plasma decomposition processes form a-SiC:H from SCB. More rapid film deposition, ~20 nm/min, is obtained by PECVD processing at temperatures as low as 150°C with a 10 volume percent silacyclobutane concentration in argon at a pressure of ~10 Pa (~0.1 torr). Figure 22 shows the schematic of the PECVD system.

Refinement of Process Parameters - High Pressure

Emphasis was placed on the development of an increased pressure plasma-SiC growth process which was expected to enhance film growth in non-planar regions. Adequate coating of non-planar regions, such as steps, overhangs, and underneath bondwire, is important for single chip and MCM substrates.

The initial higher pressure experiments were conducted with a reactor pressure of ~260 Pa (2.0 Torr). This pressure was chosen based on a review of research published in 1975-1985 on the deposition of plasma-SiN films for primary passivation applications.

Several results were obtained from these initial experiments. Compared with prior experience, the increased pressure dramatically improved the plasma confinement between the electrodes. This minimized unnecessary deposition on the reactor walls. The plasma-SiC film deposition rate varied from ~50 to 110 nm/minute, inversely proportional to the gap distance. The plate gap was adjusted to obtain a continuous discharge for the process conditions studied as this is known to produce good film quality.

The repeatability of the deposition rate was determined by coating four 100 mm wafers and performing 13 runs coating CD4011B CMOS devices, with witness wafer pieces. A consistent deposition rate of 53.1±2.0 nm/min was obtained on the wafers. The deposition rate for the witness wafers from the 13 device coating runs was 46.2±4.9 nm/min; the greater variation observed is believed due to the small wafer piece used as a witness wafer and coated with the devices. A subsequent SEM cross-section analysis was performed on three of the coated CMOS devices; the deposition rate for these devices ranged from 44.5 to 46.3 nm/min. The repeatability of the deposition rate appears to be greater than 90%.

SEM cross-sectional analyses of the three plasma-SiC coated CMOS devices showed that these higher pressure deposition conditions produced a coating in the fillet region of the bondpad and on the side of the chip. These regions are traditionally difficult to coat, due to shadowing.

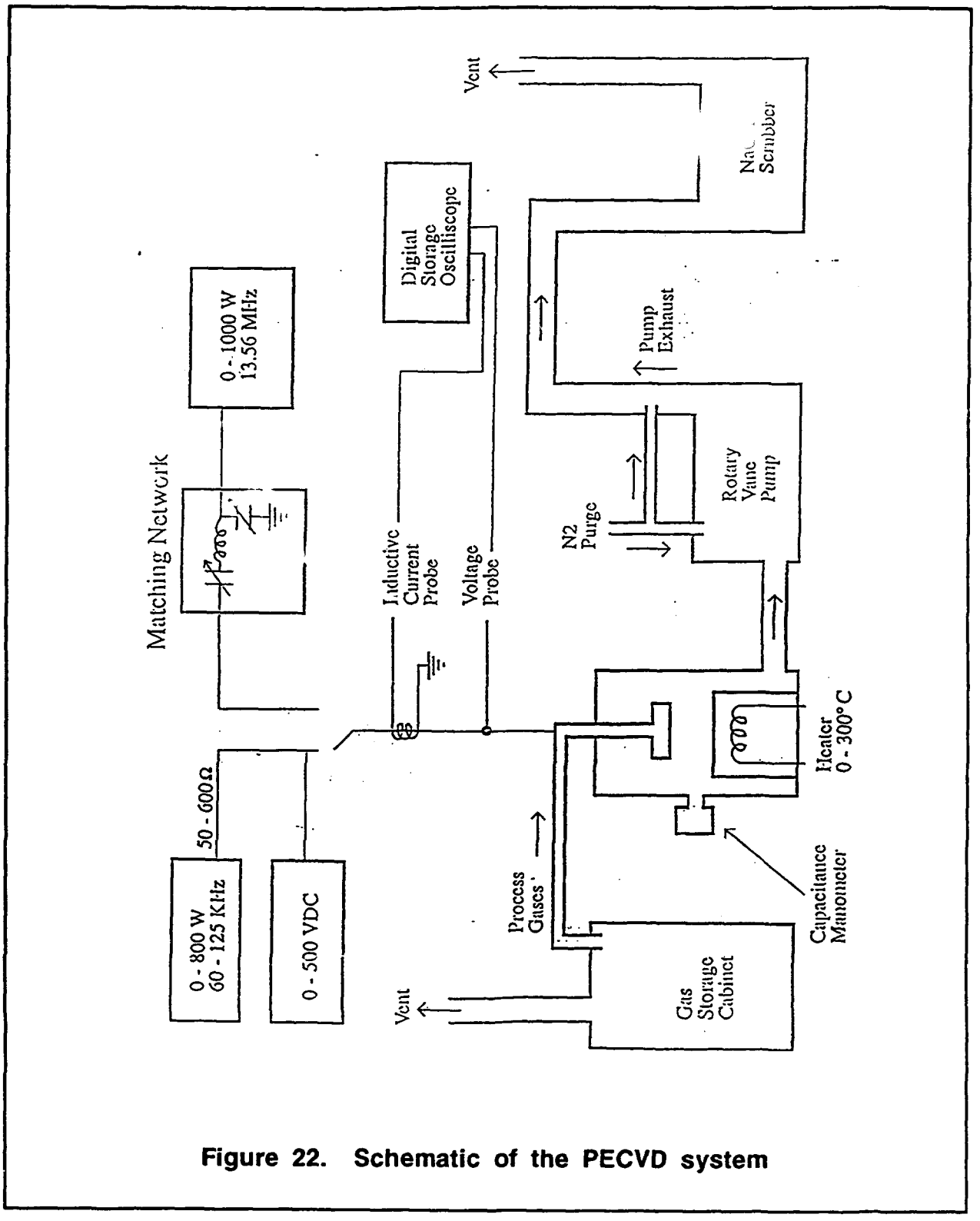


Figure 22. Schematic of the PECVD system

Carrier Gas

A comparison of carrier gases used during PECVD deposition of plasma-SiC was conducted; helium and argon were investigated. With all deposition parameters held constant, it was found that the use of argon results in better plasma confinement in the deposition area.

The use of argon as a carrier gas has three advantages. First, it minimizes particulate generation during the process, as particulates are generated by deposition of material on the cool walls of the vacuum system which will eventually flake off during processing. Second, a confined plasma provides a repeatable and efficient deposition process. Third, the use of argon also increases the deposition rate, most likely because of the better plasma confinement.

Based on these observations, and the importance of producing pinhole-free coatings, argon was used as the standard carrier gas for PECVD deposition of plasma-SiC barrier layers.

Plasma Frequency and DC Bias

Experiments were conducted to investigate the influence of plasma frequency on the properties of plasma-SiC coatings and to determine if dc biasing of the powered electrode could control the ion bombardment in a manner which affects the film properties. Silacyclobutane in argon was used; all deposition conditions were maintained constant as for typical depositions except for the plasma frequency, 0.125 or 13.56 MHz, and electrode bias.

The experiments revealed that the plasma frequency did not affect the film deposition rate at low precursor concentrations. There was less chamber sidewall deposition when using the lower plasma frequency, but the higher plasma frequency enhances the film uniformity and deposition repeatibility. The plasma current was much lower, by a factor of 500, with the lower plasma frequency and produces coatings with a consistently higher refractive index.

A comparison of the substrate temperature with plasma frequency was conducted using argon and oxygen plasma. The lower plasma frequency produced very little heating of the wafer during argon plasma and <20% increased heating in oxygen plasma. The higher plasma frequency consistently increased the heating of

the wafer by 20-30% in argon and oxygen plasma. During a silacyclobutane/argon deposition run, the wafer equilibrium temperature was increased by 20%.

Deposition of Plasma-SiC Through a Mask

For these deposition experiments, argon plasma was used at 250°C with a frequency of either 0.125 or 13.56 MHz. The deposition chamber of the parallel plate PECVD reactor uses laminar flow of the process gases to deposit uniform thin-film plasma-SiC coatings. The use of a shadow mask places a large metal step near important coating areas which severely limited the deposition of the coating near it. Large inhomogeneities in material and deposition characteristics were found within a film from an individual mask opening. Film thickness varied by 50% across the opening, independent of deposition conditions.

These problems were sufficiently reduced by enlarging the mask opening by ~100% of the important coating region, reducing the mask thickness, and increasing the gas flow rate to slightly decrease the deposition rate. Film thickness variations of ~10 to ~20% were now typical as shown by Figure 23. The PECVD masking template for the CD4011B is shown in Figure 24 and the template for the LM124 is shown in Figure 25.

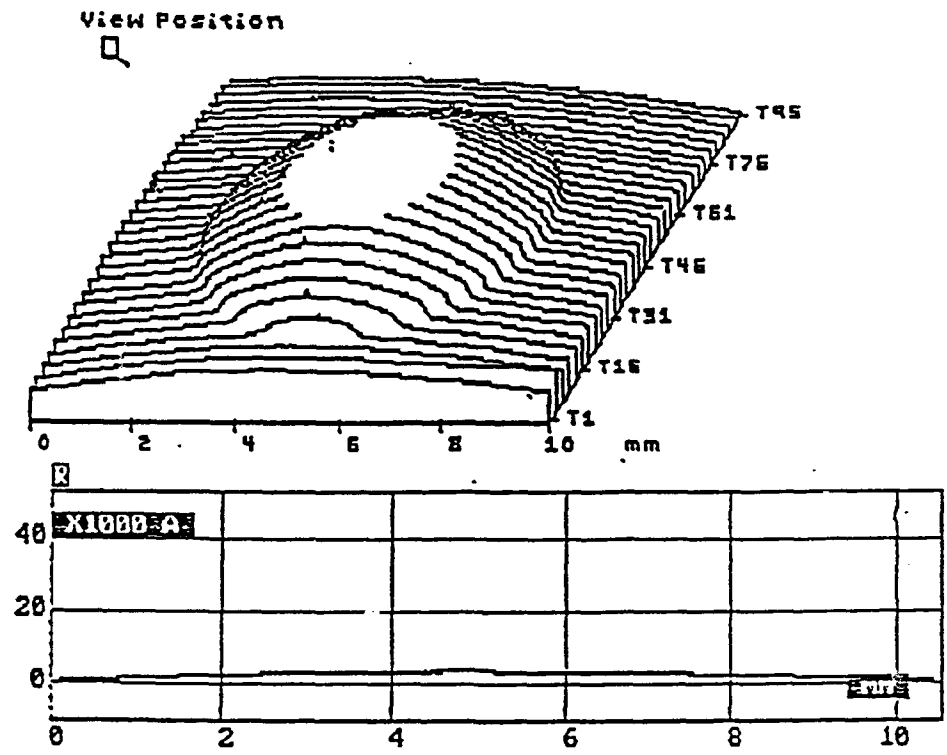
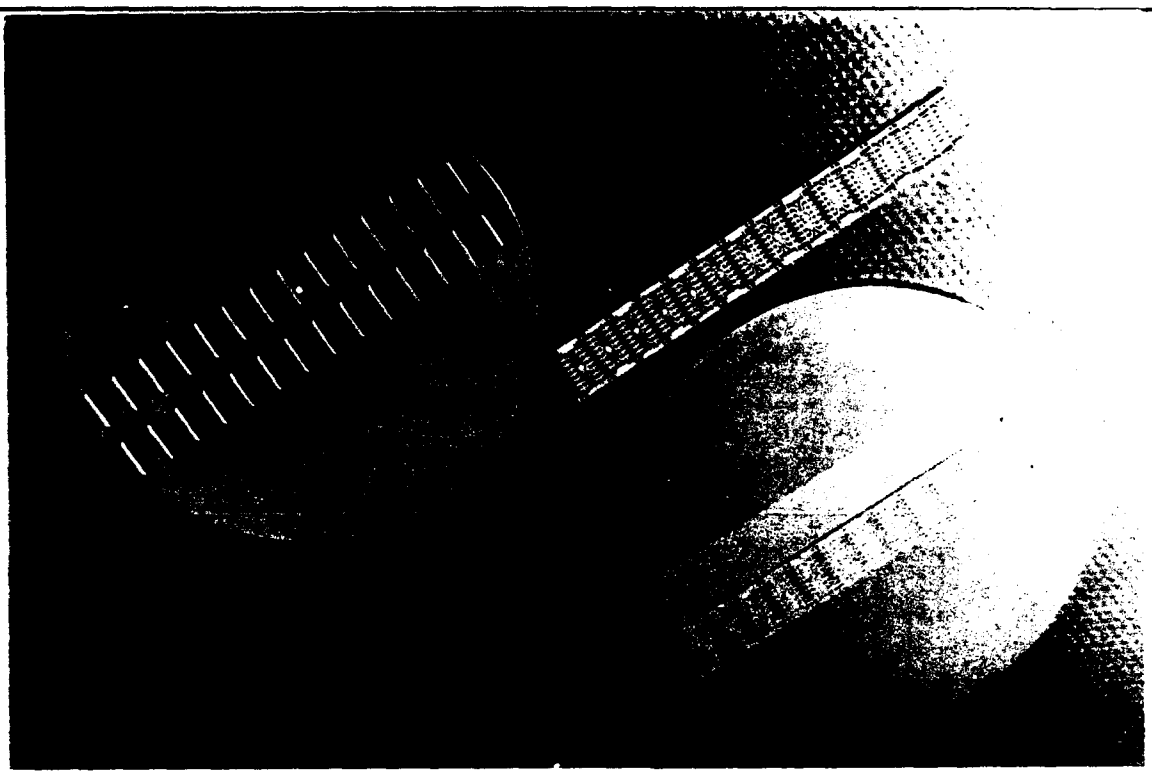
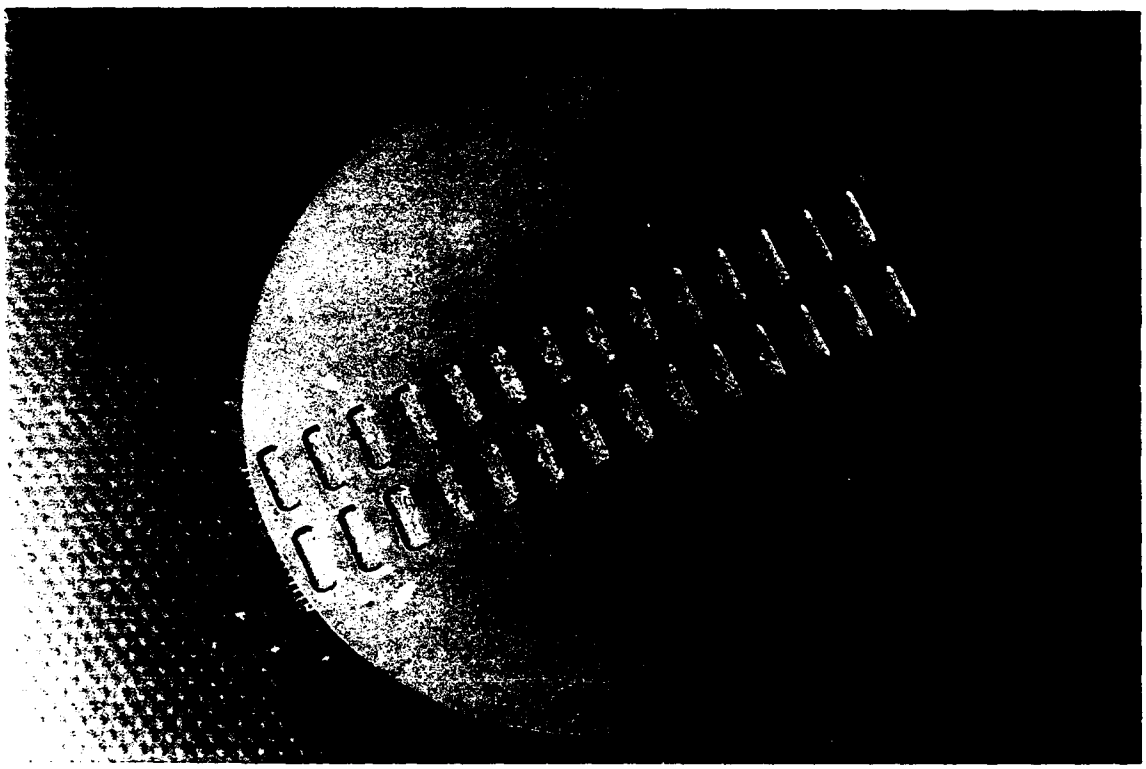


Figure 23. Topography of plasma-SiC coating deposited using improved shadow mask and deposition conditions.

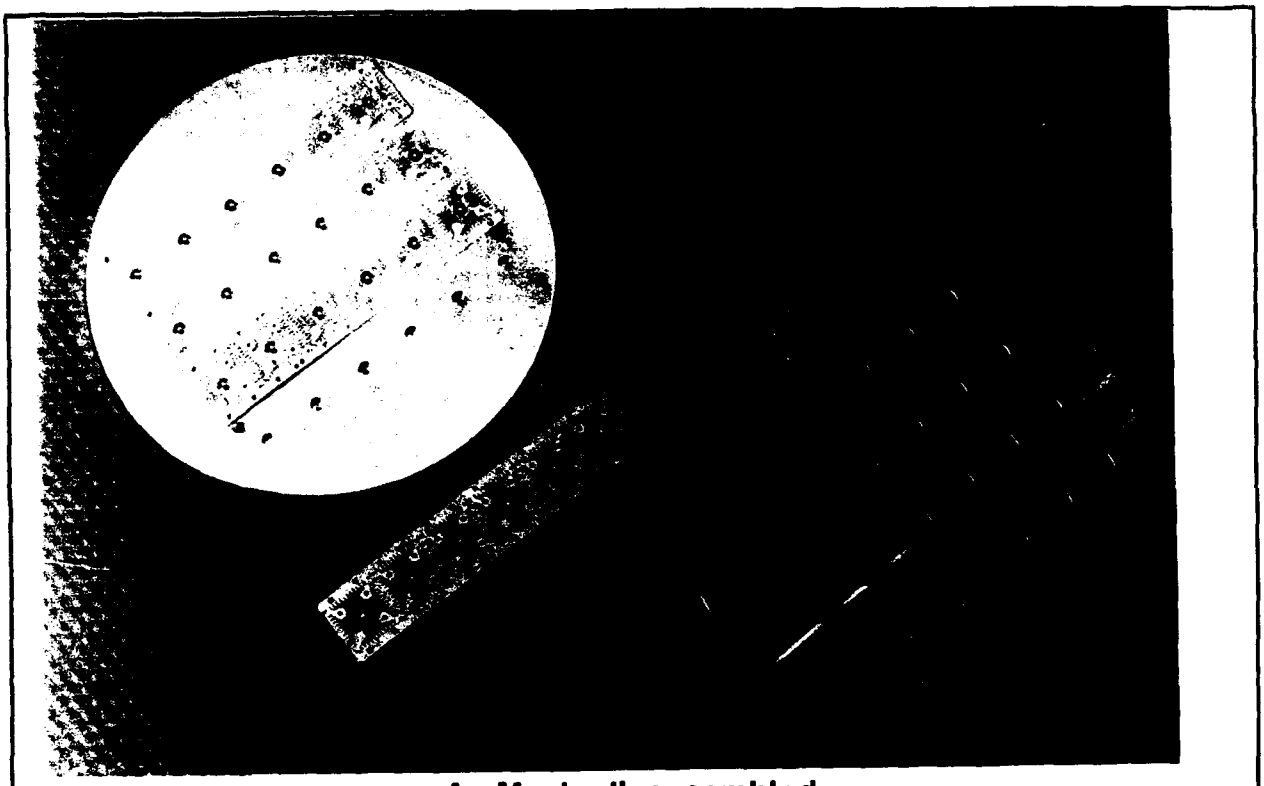


A. Mask disassembled.

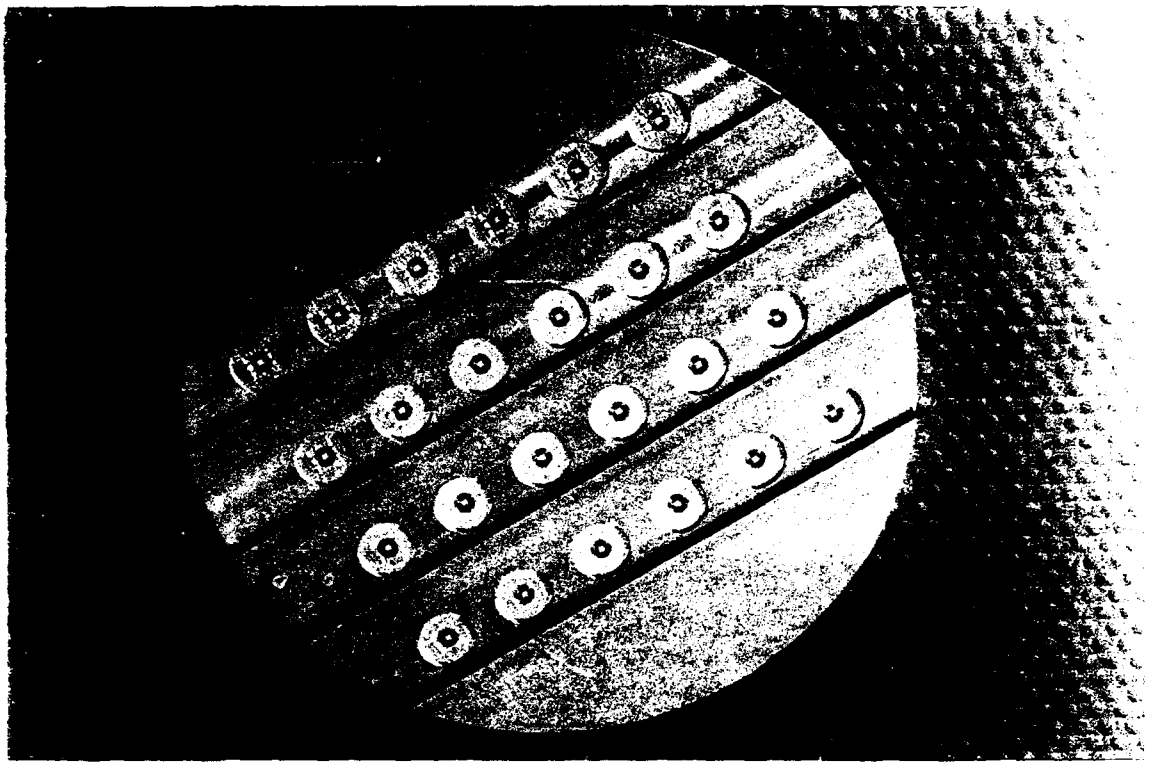


B. Mask assembled.

Figure 24. PECVD masking template for a CD4011B leadframe.



A. Mask disassembled.



B. Mask assembled.

Figure 25. PECVD masking template for a LM124 TapePak™.

Characterization of Plasma-SiC Coatings

The mechanical, electrical, and morphological properties of the silacyclobutane derived plasma-silicon carbide film at 250°C are summarized in Table 3 [11].

Table 3. Characteristics of Plasma-SiC Films Processed at 250°C.

Mechanical	
Stress (MPa)	300 (C)
Elastic Modulus (GPa)	~ 100
Hardness (GPa)	15.4
CTE (ppm/°C)	3.0
Density (g/cm^3)	1.7 - 2.0
Electrical/Optical	
Dielectric Constant	4 - 6.2
Loss Factor	< 0.005
Volume Resistivity (ohm-cm)	$>10^{12}$
Dielectric Strength (V / μm)	--
Refractive Index	1.9-2.3
Microstructural/Morphological	
Composition: (C:Si)	1.4 - 2
Pinholes (Glassivation Test)	Pass
Density (g/cm^3)	1.7 - 2.2

Established PECVD Process for Barrier Layer

Based on the results of process experiments and analysis obtained in this program, a standard PECVD process was established for applying the plasma-SiC barrier layer on devices. Cross sections of coated CMOS devices showed that good coatings are produced in the fillet regions of bondpads, center of the die, and on the side of chip, regions traditionally difficult to coat. Figure 26 shows the coating coverage afforded by the applied silicon dioxide and plasma-SiC in the central die and ILB regions.

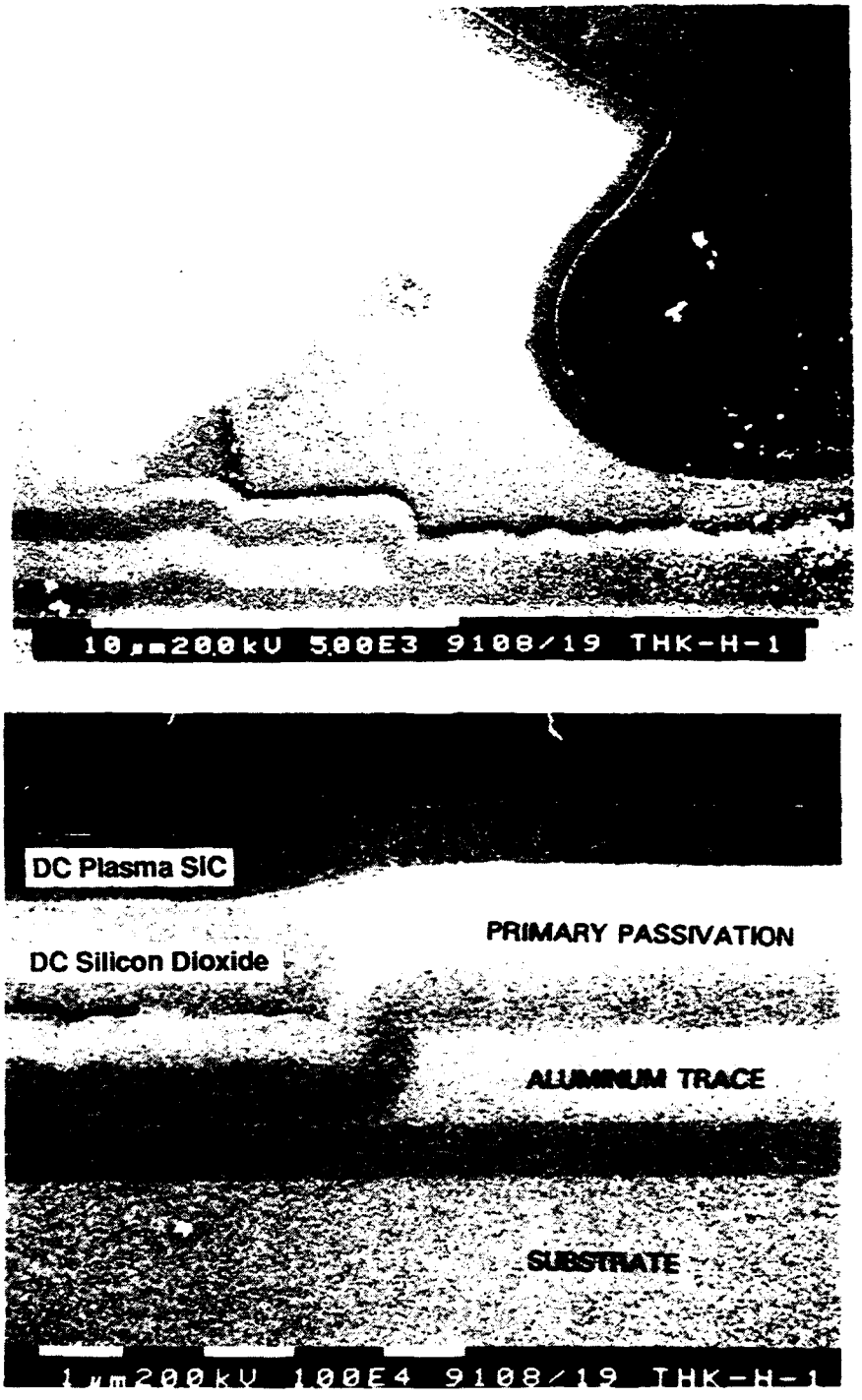


Figure 26. Coverage of the SiO_2/plasma-SiC ceramic coatings on an interior circuit region and inner lead bond.

Stress in Ceramic Coatings

The mechanical stresses in the silicon dioxide, plasma-SiC, and dual-layer coatings were studied to improve the understanding of the characteristics of these films. The intrinsic stress was measured by changes in wafer curvature after ceramic coating application and following temperature cycling and autoclave exposures.

The results show that prior to environmental stress exposure, the silicon dioxide coatings were under a tensile stress, 100-200 MPa ($1\text{-}2 \times 10^9$ dyne/cm^2). The stress increased by a factor of 1.2 to 2.0 (thickness dependent) after the initial 100 temperature cycles of -65 to 150°C, but changed very little with subsequent temperature cycles.

The plasma-SiC coatings were under a compressive stress, ~300 MPa ($\sim 3 \times 10^9$ dyne/cm^2), prior to temperature cycling. This stress increased by a factor of 1.5 to 2.0 (thickness independent) after the initial 100 temperature cycles but again there was very little change with subsequent cycles.

The net stress in the silicon dioxide/plasma-SiC dual-layer coating was small, <50 MPa. For a 100 nm thick silicon dioxide layer and a 370 nm thick plasma-SiC layer, the net stress was in tension, while for a 700 nm thick plasma-SiC coating, the stress was compressive. In both cases, the net stress became compressive after the first 100 temperature cycles.

No peeling, cracking or flaking of the coating was observed. The change in the stress in the silicon dioxide layer with temperature cycling indicates moisture may be released since moisture tends to reduce stress. The behavior of the dual-layer coating mimics the carbide layer by itself. The plasma-SiC layer prevents moisture from reabsorbing in the silicon dioxide.

These results indicate the silicon dioxide/plasma-SiC coatings are relatively insensitive to temperature cycling. The changes measured after the first 100 cycles were close to the sensitivity level of the instrument, ± 10 MPa ($\pm 0.1 \times 10^9$ dyne/cm^2).

Adhesion of Epoxy Molding Compound to Plasma-SiC

It has been reported that the adhesion of an epoxy molding compound (EMC) to the IC primary passivation (plasma-SiN) and leadframe is of prime importance for reliable plastic encapsulated devices [12]. Separation or voiding at this interface may provide a site for condensing water vapor or moisture resulting in the corrosion of circuit metallization.

Questions regarding the adhesion of NSC's conventional EMC to the plasma-SiC coating and whether the high stress of the EMC would degrade the integrity of the dual-layer ceramic coatings were addressed. Scanning acoustic microscopy (SAM) and cross-sectional analysis were used to assess the interfaces between the EMC and the ceramic coatings. In these experiments, actual test devices with and without the dual-layer ceramic coatings were used with their appropriate EMCs. Test sample plastic encapsulated devices were compared as molded, after 100 hours of autoclave at 121°C, 100% RH, and after 100 temperature cycles at -65 to 150°C.

CD4011B Test Device

The conventional EMC used on the CD4011B CMOS device was Nitto MP101S, used in accordance with standard transfer molding processes at NSC; this included a six hour post-mold cure at 175°C.

No difference in adhesion was observed between the plastic encapsulated devices with a standard (uncoated) die and those with the ceramic coating regardless of whether they were exposed to autoclave or temperature cycling conditions. Adequate adhesion of the EMC to the ceramic coatings was revealed by SAM and confirmed by cross-sectional SEM. Good adhesion was also observed between the silicon dioxide and plasma-SiC layers, and between the silicon dioxide and existing primary passivation (plasma-SiN).

LM124 Test Device

The conventional EMC used on the LM124 Op-Amp device was Sumitomo 6300 low stress compound, used in accordance with standard injection molding processes at NSC; this included a four hour post-mold cure at 175°C.

Again, no difference in adhesion was observed between the plastic encapsulated devices with a standard (uncoated) die and those with the ceramic

coating regardless of whether they were exposed to autoclave or temperature cycling conditions. Adequate adhesion of the EMC to the ceramic coatings was revealed by SAM. Good adhesion was also observed between the silicon dioxide and plasma-SiC layers, and between the silicon dioxide and existing primary passivation (plasma-SiN).

Based on these results, it was shown that the low-temperature ceramic coatings were compatible with the materials and processes used in the molding of both the CMOS and Op-Amp devices. The integrity of the ceramic coatings were not adversely affected by the high mechanical stress induced by the molding compound even after autoclave or temperature cycling exposures.

APPLICATION OF CERAMIC-COATED TEST VEHICLES

Application techniques to provide continuous coverage of the solution applied silicon dioxide smoothing layer to a leadframe chip carrier were assessed. Ultrasonic spray application was found to provide good coverage on the circuit assembly. The remaining processes used for applying the inorganic coatings were derivations of standard semiconductor fabrication techniques which were tailored to leadframe applications. Typical thicknesses of the applied transparent films were 200-300 nm for the silicon dioxide and 600-700 nm for the plasma-SiC layers.

Application of Ceramic Coatings to Test Devices

The following process was used for preparation and coating of the CD4011B and LM124 leadframes, LM124 chip-on-tape, and CD4011B open cavity sidebrazed package devices in this program. Silicon wafer pieces were used as process monitors during the coating process. Infrared spectroscopy (FTIR) was used to assess the complete conversion of the precursor to SiO_2. The dual-layer ceramic coatings were assessed by optical inspection, bond pull strength, and glassivation tests when possible.

Preparation / Cleaning:

The leadframe strips or packaged devices were thermally conditioned at 250°C in nitrogen for 0.25 hour. The devices were then vapor cleaned using isopropanol to remove loose particles and subsequently exposed to an UV / ozone cleaning system (UVOCS) for 0.25 hour to remove residual isopropanol solvent and organic contaminants from the substrate.

Silicon Dioxide Smoothing Layer:

Immediately after cleaning, the strips of devices were placed into spray coating shadow masks which permitted the application of the hydrogen silsesquioxane solution only to the die and frame interconnect regions. The silicon dioxide layer was produced from a 10 wt% hydrogen silsesquioxane solution in dimethylcyclosiloxane (HIPEC Q2-1345) which was applied by ultrasonic spray, exposed to 200°C in nitrogen to accelerate solvent removal and provide thin film flow, and converted to silicon dioxide using an ammonia/steam process at 250°C. The typical thickness of the silicon dioxide layer was 300 nm.

Plasma-Silicon Carbide Barrier/Passivation Layer:

The plasma-SiC barrier layer was produced using silacyclobutane as the precursor and applied by PECVD. A shadow mask was used to deposit the plasma-SiC coating to specific regions of the die and interconnect regions. The die temperature during deposition was measured during the process development and was maintained at 250°C. Typical thickness of the plasma-SiC layer was 600-700 nm.

Assessment of Ceramic Coatings

Three quality assurance procedures were employed on the coated leadframes strips and packaged devices: optical inspection, bond pull strength, and glassivation tests. These tests were performed in accordance with MIL-STD-883D, Methods 2010, 2011 Cond. D, and 2021 respectively.

The optical inspection was coordinated during the coating process to provide feedback for continuous improvement of the operation. A 100% lot acceptance inspection was performed on all coated devices to remove any die or assembly-related conditions, handling damage, coating defects, or other anomalies.

CD4011B Leadframes

Dual-layer ceramic coatings were applied to partially assembled CMOS die on leadframe chip carriers. The assembly consisted of a nickel plated copper leadframe (13 mil thick) with a gold spot, and used silver filled polyimide die attach and had 1.25 mil diameter gold leadwires (thermosonic ball bond on die, crescent bond on frame).

The lot acceptance rate of the coated CD4011B devices was approximately 88%. Optical inspection of the die and interconnect regions at 100 to 400X magnification revealed very good coating coverage, minimal particulates, and good adhesion to the die (including the sides), bondpads, and gold spot plating. Random cracking and flaking was observed on the gold leadwires. Figure 27 displays a dual-layer ceramic-coated CMOS device on a leadframe chip carrier. The rainbow appearance of the ceramic coatings on the leadframe is due to variations in the submicron thickness of the plasma-SiC coating revealed by light interference fringes. The thickness variations are caused by the shadow mask during the coating deposition as discussed previously in this report.

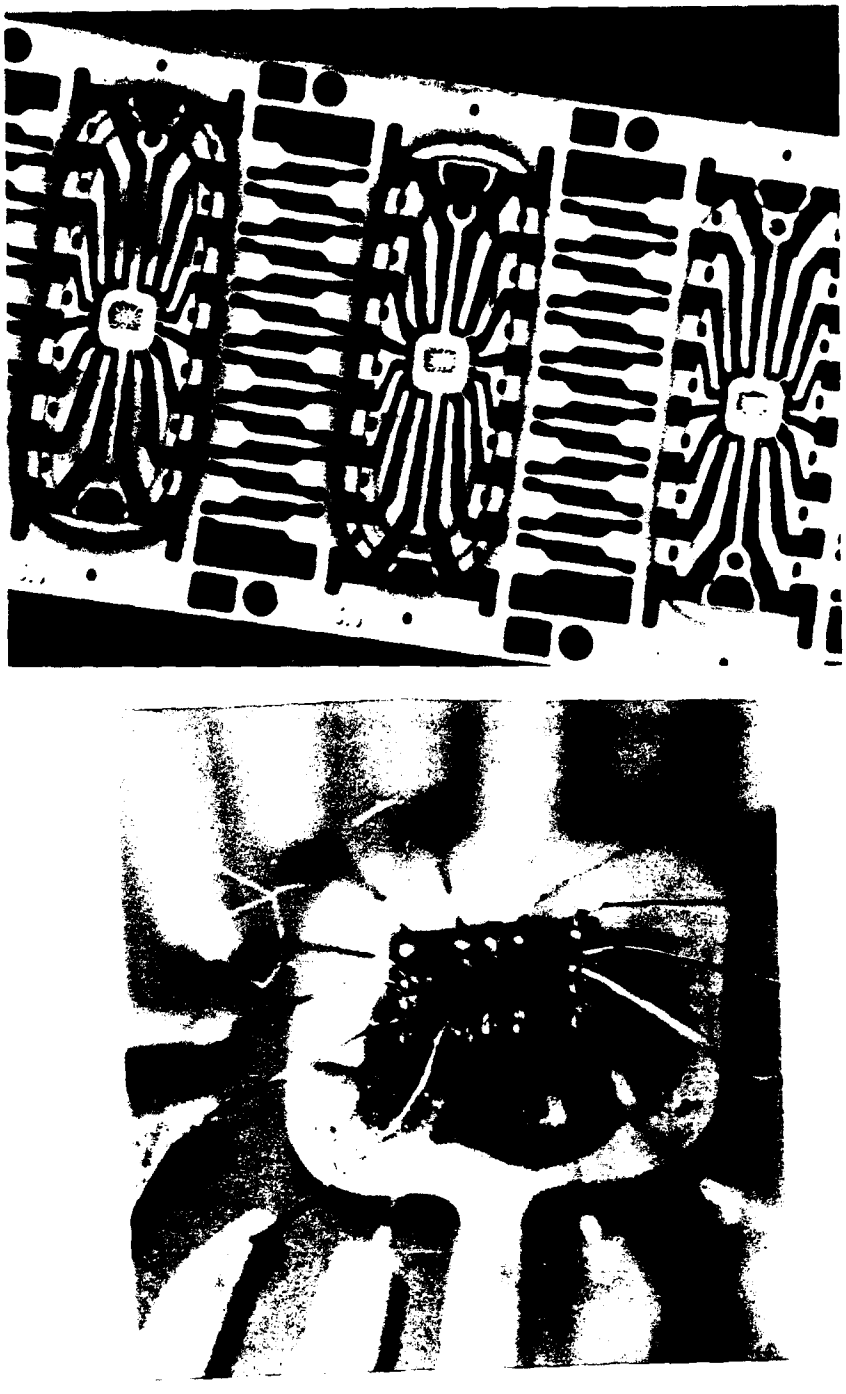


Figure 27. Appearance of a ceramic-coated CMOS device on a leadframe prior to plastic overmolding.

Bond pull strength tests were completed on both standard (uncoated) die and ceramic-coated die leadframes. A slight reduction in bond pull strength was observed; 13 $\pm$ 1.6 grams reduced to 12 $\pm$ 1.2 grams respectively. No variation in the leadwire break location was observed after the ceramic coating process; the leadwire break location was at the neckdown to bond pad region. Compilation of the bond pull strength data may be found in Appendix C.

Glassivation testing per MIL-STD-883D verified the complete sealing of aluminum bondpads by the ceramic coatings. All sampled parts tested passed the extended exposure to the glassivation test and moreover, demonstrated bond pad protection for up to 15 hours of glassivation exposure. Standard die had complete dissolution of the aluminum bond pad within 0.25 hour.

The completed CD4011B leadframes were hand carried to National Semiconductor's South Portland, Maine facility for plastic molding. Incoming inspection on a random sampling revealed peeling of the coating on some gold wires. Standard molding materials and processes were used; Nitto MP101S epoxy compound was used in a transfer molding process. Each mold accommodated 2 leadframe strips, one uncoated and one ceramic-coated leadframe, which were readily distinguishable by leadframe markings. The molded leadframes were subjected to a six-hour post-mold cure at 175°C followed by lead trim and form, solder dip, and marking.

The ceramic-coated die leadframes resisted the standard lead finish procedure due to surface oxidation of the leadframe. A variety of chemicals and procedures were tried for removing the surface oxidation; freon, methanol, isopropanol, copper etchant solution, extra time in standard flux, and a dip in 50% H_2SO_4 solution. The final cleaning solution was a 20 minute immersion in 140°C Kester "Solder-Nu" metal cleaner (formula 5560) followed by a deionized water rinse. Approximately 40 units were solder-dipped by multiple dipping, the balance were processed through the Kester process.

To ensure standardization of experimental units, the 40 units exposed to multiple solder dips plus an additional 10 units from the Kester process were used for the data item deliverables submitted to Wright Laboratory. All of the ceramic-coated die in plastic packages were processed in the same manner and were used in the reliability test program.

LM124 Chip-on-Tape

Dual-layer ceramic coatings were applied to partially assembled die on copper tape (chip-on-tape). The assembly consisted of 3 mil copper tape (with bumped tape) interconnected using TAB where the die was below the plane of the tape.

The lot acceptance rate of the coated LM124 devices was approximately 70% due to intermittent particle problems. Inspection of the LM124 devices revealed random discoloration of the gold capped bond pad which was not observed during previous coating activity. Visual inspection of gold capped bond pads on coated LM124 devices revealed random color changes from metallic gold to gray, indicative of intermetallic formation between copper and gold. Figure 28 displays a dual-layer ceramic-coated chip-on-tape Op-Amp device.

Other observations of the coated LM124 devices revealed moderate adhesion of the ceramic coatings to the copper tape; inconsistent adhesion was observed primarily on the bonded region of the tape which is secured to the chip. It is suspected that oxidation of the copper from the thermocompression bonding weld resulted in a reduction of adhesion.

Bond pull tests were not performed due to limitations of DCC's equipment. The glassivation test did not reveal any useful data on how well the coating sealed the gold bond pads.

The completed LM124 chip-on-tape was hand-carried to National Semiconductor's Santa Clara Packaging Pilot Line for molding and end-of-line processing. Standard TapePak™ materials and processes were used. Sumitomo 6300 Low Stress molding compound was used in a transfer molding operation by strips consisting of six units each. A four-hour post-mold cure at 175°C was used.

LM124 Leadframes

Dual-layer ceramic coatings were applied to partially assembled linear Op-Amp die on leadframe chip carriers. The assembly consisted of a nickel plated copper leadframe (13 mil thick) with a gold spot, and used silver filled polyimide die attach and had 1.25 mil diameter gold leadwires (thermocompression ball bond on die, crescent bond on frame).

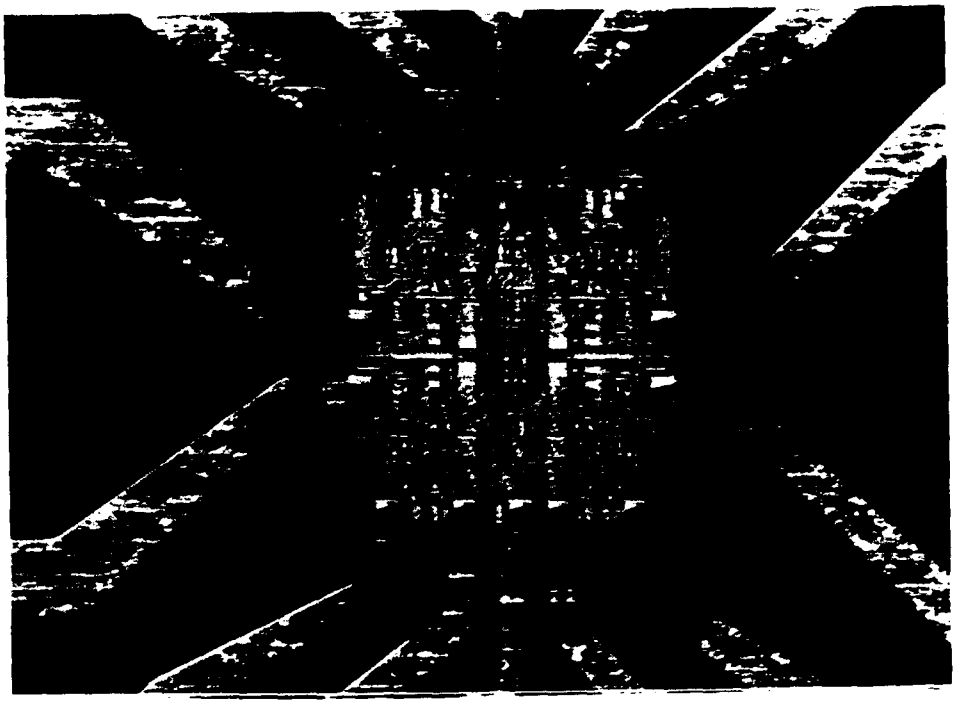


Figure 28. Appearance of a ceramic-coated chip-on-tape linear Op-Amp device prior to plastic overmolding.

The bond pad metallization of the LM124 devices used on a standard 14-lead DIP leadframe assemblies are aluminum and were not processed through NSC's bump fabrication like those prepared for chip-on-tape (TAB). Thus the assembly of the LM124 on standard leadframes approximates that used for the CD4011B; the only difference was the epoxy molding compound. It was expected that the use of these LM124 devices could provide process compatibility data in the event that the observations made on the coated chip-on-tape devices reduces the performance in the long term reliability test program at NSC.

The lot acceptance rate of the coated LM124 devices was approximately 38% due to foreign contamination (dirt particles) and cracking of the coating on damaged wire bonded aluminum pads. Optical inspection of the ceramic-coated die and interconnect regions revealed very good coating coverage and good adhesion to the die (including the sides), bondpads, and gold spot plating. Random cracking and flaking was observed on the gold leadwires and some random cracking on the

damaged bond pads. Figure 29 displays a dual-layer ceramic-coated linear Op-Amp device on a leadframe chip carrier.

No bond pull strength testing was performed due to the limited quantity of leadframe devices submitted for coating. The glassivation test per MIL-STD-883D was used to verify that complete sealing of the aluminum bond pads was accomplished. A sampling of both standard die and ceramic-coated die were tested. All standard die showed complete dissolution (removal) of the aluminum bond pads within 0.25 hour and all ceramic-coated devices tested passed a 15 hour glassivation acid test exposure.

CD4011B Ceramic Sidebrazed Packages (D-Packages)

Dual-layer ceramic coatings were applied to CMOS die assembled in ceramic open cavity sidebrazed packages (D-packages) with eutectic die attach and had 1.25 mil diameter aluminum leadwires.

The lot acceptance rate of the coated CD4011B devices was approximately 82%. Optical inspection of the ceramic-coated die assembled in D-packages also revealed good coating quality. Complete coverage was achieved on the die (including the sides of the die), aluminum leadwires, and frame post regions. Figure 30 displays a dual-layer ceramic-coated CMOS device in an open cavity sidebrazed package.

Bond pull strength testing of both standard die and ceramic-coated die revealed a reduction in strength; 10 $\pm$ 2 grams reduced to 6 $\pm$ 0.9 grams. However, all devices met the minimum bond pull strength requirement specified in MIL-STD-883D Method 2011. The reduction in bond pull strength could be attributed to the annealing of aluminum wire at 250°C. The variance of bond pull strength was improved after the coating processes. No significant difference in leadwire break location was observed (neck down to die region) between the standard (uncoated) die and the ceramic-coated die. All of the bond pull strength data may be found in Appendix C.

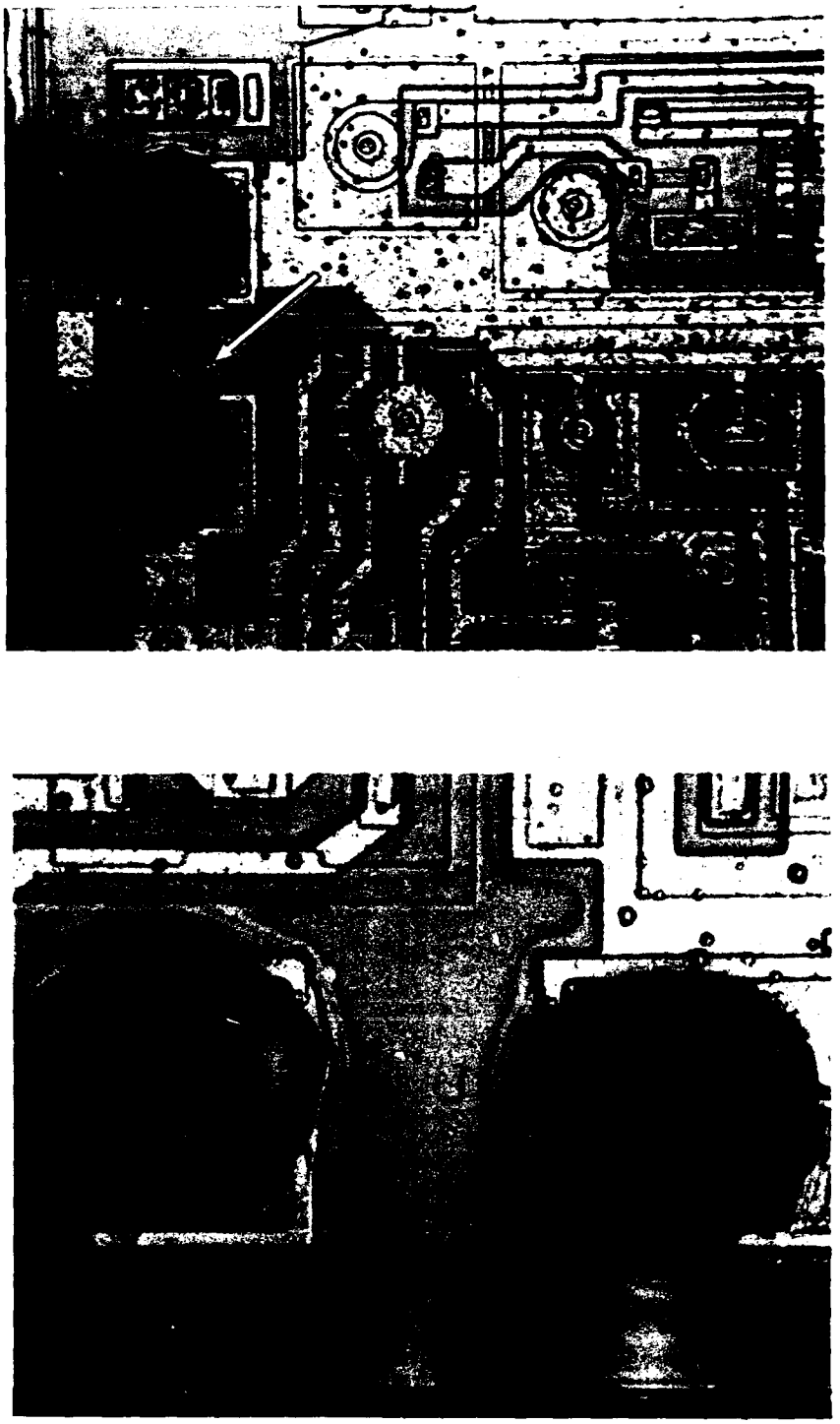


Figure 29. Appearance of a ceramic-coated linear Op-Amp device on a leadframe chip carrier prior to plastic overmolding.

The glassivation test per MIL-STD-883D was used to verify that complete sealing of the aluminum bond pads was accomplished. A sampling of both standard die and ceramic-coated die were tested. All standard die showed complete dissolution (removal) of the aluminum bond pads within 0.25 hour and all ceramic-coated devices tested passed a 15 hour glassivation acid test exposure.

Electrical Testing

Full electrical (parametric) testing was performed on the LM124 Op-Amp and CD4011B CMOS devices. An example of the test parameters may be found in Appendix D.

High electrical device yields (>98%) were achieved on the experimental ceramic-coated CD4011B and LM124 die in plastic packages (PDIPs and TapePak™); equal to standard (uncoated) die in similar packages. The same high electrical device yields (>98%) were also achieved on the ceramic-coated CD4011B die assembled in D-packages; this yield equals that of standard (uncoated) die in similar packages.

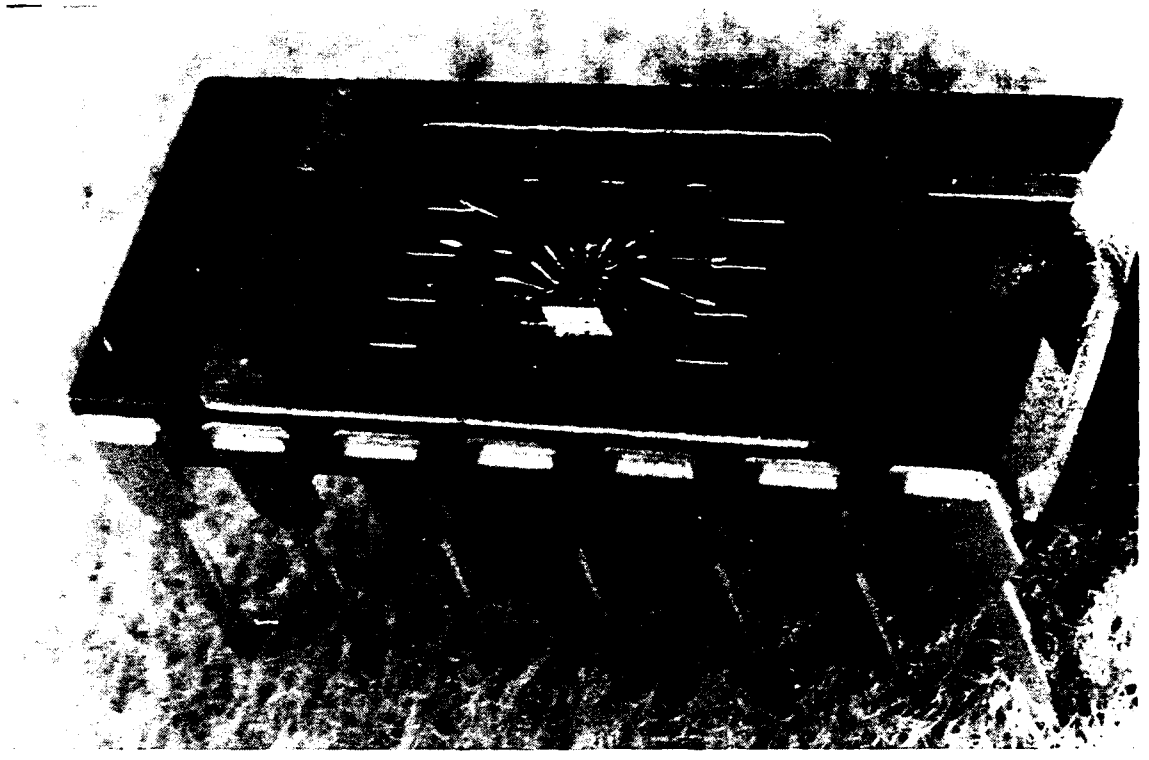


Figure 30. Appearance of a ceramic-coated CMOS device in a ceramic open cavity sidebrazed package.

RELIABILITY TESTING

A variety of severe and differentiating environmental exposures were used to assess the reliability of commercial state-of-the-art plastic packaged devices for military products. Well understood and robust devices, CD4011B CMOS and LM124 Op-Amp, were packaged in PDIP and TapePak™ technologies using standard commercial practices. Ceramic-coated die were integrated into existing commercial plastic packaging, subjected to environmental exposures, and assessed with respect to standard (uncoated) commercial devices. Comparative reliability data will be made against standard die in traditional hermetic packages. Additionally, the reliability of ceramic-coated CD4011B bare die in chip carriers was assessed with respect to standard die for correlation with future MCM insertion.

Device failures were defined as an open circuit, short, or irreversible parametric shift attributable to ion or moisture induced circuit degradation. Examples of conditions not considered failures include electrostatic discharge (ESD), electrical overstress (EOS), package-related leakage current, board assembly (solder) degradation, etc.

CD4011B CMOS Device

A description of the test device configurations referred to throughout the reliability testing and failure analysis sections of this report are as follows:

(Plastic & Hermetic)

Abbreviation	Description
Standard PDIP	Standard die (no die coat) in plastic packages.
Coated PDIP	Ceramic-coated die in plastic packages.
Control	Standard die in hermetically sealed packages.

(No Plastic)

Abbreviation	Description
Std D-packages	Standard die in open cavity side brazed packages tested with no lid.
Coated D-packages	Ceramic-coated die in open cavity side brazed packages, tested with no lid.

The reliability testing consisted of four main environmental exposures used individually or sequentially:

Autoclave [13]:	JEDEC-STD No. 22B, Method A102-A (121°C, 100% RH, 1 ATMG)
HAST [13]:	JEDEC-STD No. 22, Method A110 (157±2°C, 85% RH, 4 ATMG, 10 V)
Temp Cycle [14]:	MIL-STD-883D, Method 1010.7, Test Condition C (-65 to 150°C, 1 hr per cycle)
Salt Fog [14]:	MIL-STD-883D, Method 1009.8, Test Condition A (35°C, 0.5% NaCl, inclined 15° from normal)

A detailed description of the environmental test chambers used in this study can be found in Appendix E.

In order to achieve a closer approximation to service related performance conditions on the CMOS devices, a parallel reliability test scheme was developed with Rome Laboratory (RL) by splitting each device configuration into two groups; one group (Sequence A) was exposed directly to environmental testing while the second group (Sequence B) was pre-conditioned immediately before environmental exposure to provide sequential reliability data. Sequential testing combines moisture (absorption, ingress) with mechanical stresses (thermal, flexure, fatigue, and vibration). The reliability testing for the CD4011B CMOS device is shown schematically in Figure 31.

Statistical quantities of CMOS devices were subjected to preconditioning exposure which consisted of 24 hours autoclave (121°C, 100%RH, 1atmg) and 200 temperature cycles (-65 to 150°C). Devices passing the preconditioning exposure and the balance of unconditioned devices were subdivided and subsequently exposed to either autoclave, HAST, or temperature cycling/salt fog for sequential or direct reliability testing respectively. All devices were randomly selected for environmental testing. At the prescribed intervals, the devices were removed from the chamber and allowed to set in a nitrogen purge desiccator for 24 hours prior to full electrical testing

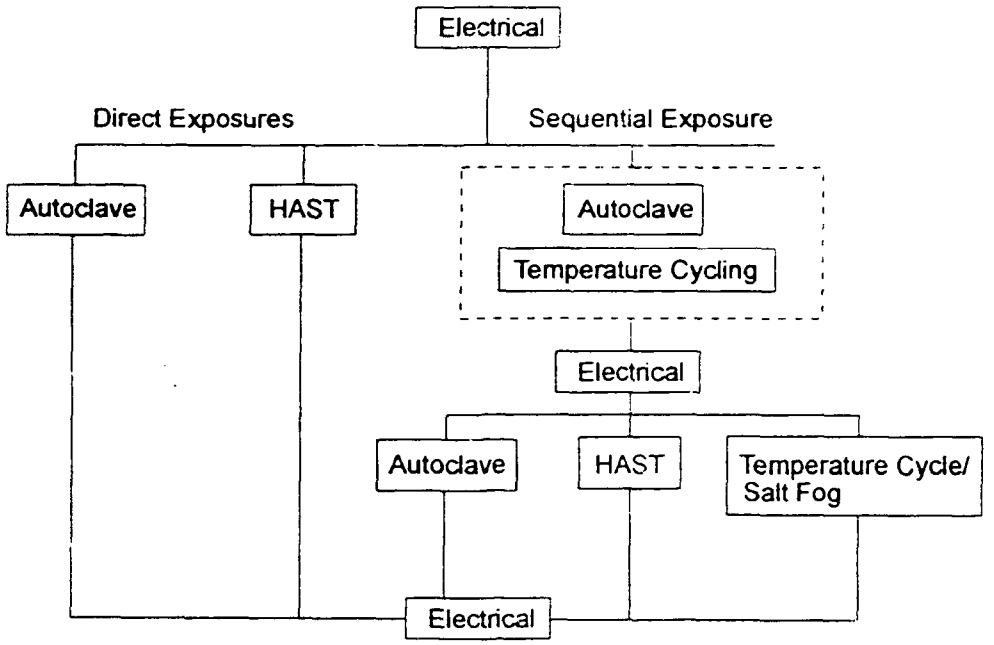


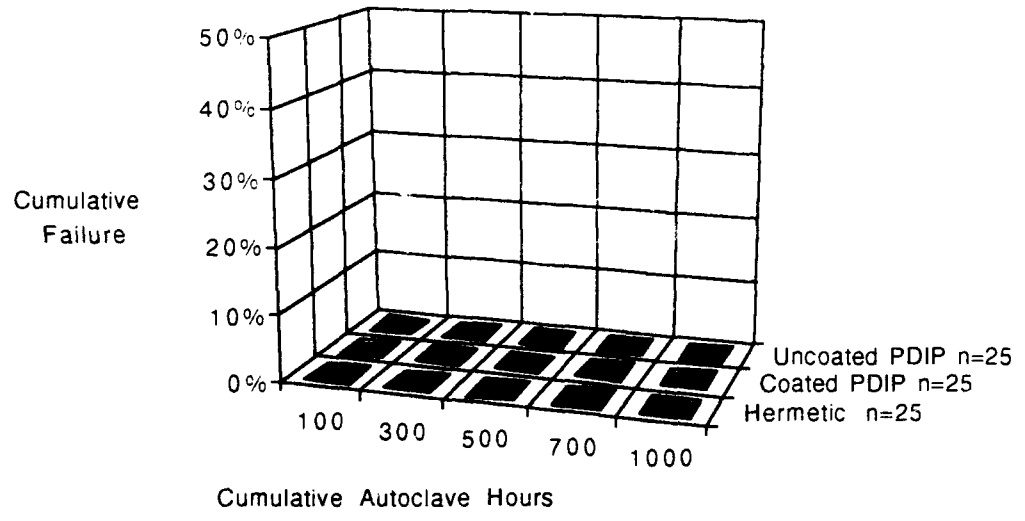
Figure 31. Reliability Test Protocol

Plastic and Hermetic Packaged CMOS Devices

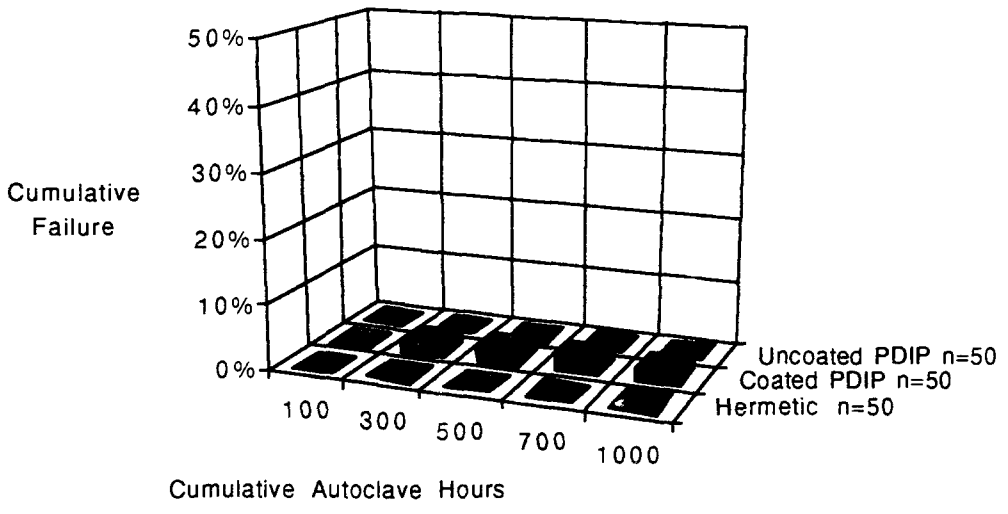
The performance results, derived from the electrical (parametric) testing on all device configurations were tabulated. The results from the reliability testing will be presented by first, comparing the reliability and failure analysis of standard commercial die (no die coat) in plastic packages against ceramic-coated die in plastic along with the hermetic control group, and secondly by comparing the reliability and failure analysis of standard bare die (no die coat) in D-packages tested with no lid against ceramic-coated die in similar packages.

Autoclave Exposure

Reliability test results from direct autoclave exposure (Sequence A) and sequential autoclave testing (Sequence B) are shown in Figure 32. The autoclave data clearly indicates that the reliability of coated PDIPs was equal to the reliability of standard PDIPs and hermetic controls. The application of the low-temperature ceramic coatings did not adversely affect the electrical performance of the integrated circuit even after 1000 hours of autoclave exposure.



(a) Direct Autoclave



(b) Sequential Autoclave

Figure 32. Reliability data of CD4011B Devices from autoclave testing.

Failure analysis of the one failed device, a ceramic-coated die in a plastic package, which was decapsulated using red fuming nitric acid revealed multiple bondpad corrosion. A photograph of the failed device is shown in Figure 33.

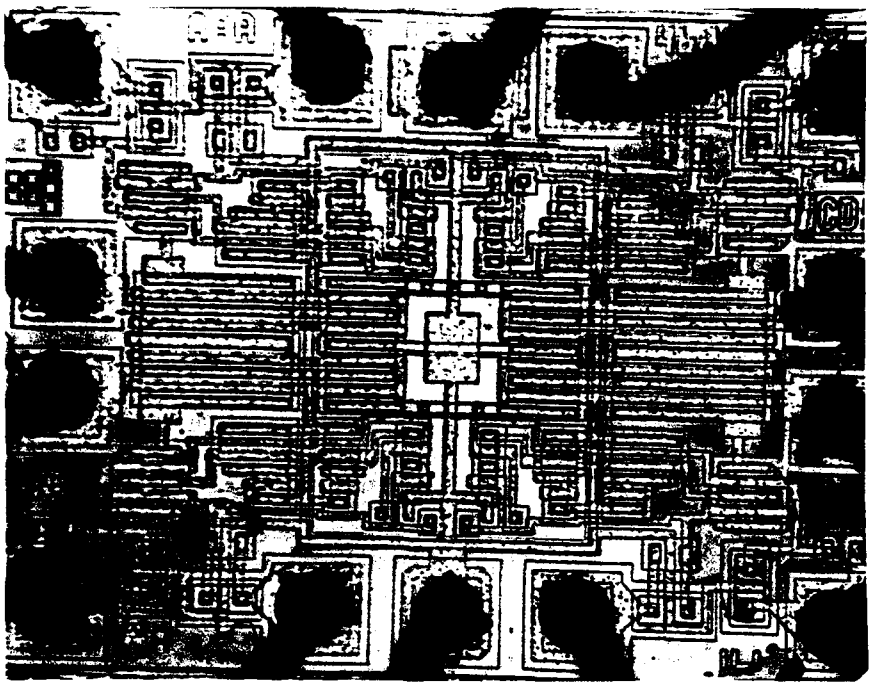


Figure 33. Photograph showing the total die of a coated PDIP after 300 hours of sequential autoclave exposure (s/n 051) 100X.

Fully functional standard and coated PDIPs, after exposure to 1000 hours of sequential autoclave, were randomly selected and analyzed for visual comparison of the aluminum bond pad metallization. The standard PDIPs revealed initial signs of ongoing uniform bond pad degradation while the coated PDIPs were completely free of any visible degradation. Representative photographs comparing standard die and ceramic-coated die after plastic decapsulation are shown in Figure 34. Scanning Auger Microscopy (SAM) analysis did not detect halogens at the bond pad interface. Based on the cumulative reliability data, both functional device performance and visual examination of passing devices, it's clear that the coated PDIPs were not affected by the sequential autoclave exposure and provided a good barrier to moisture induced bond pad degradation.

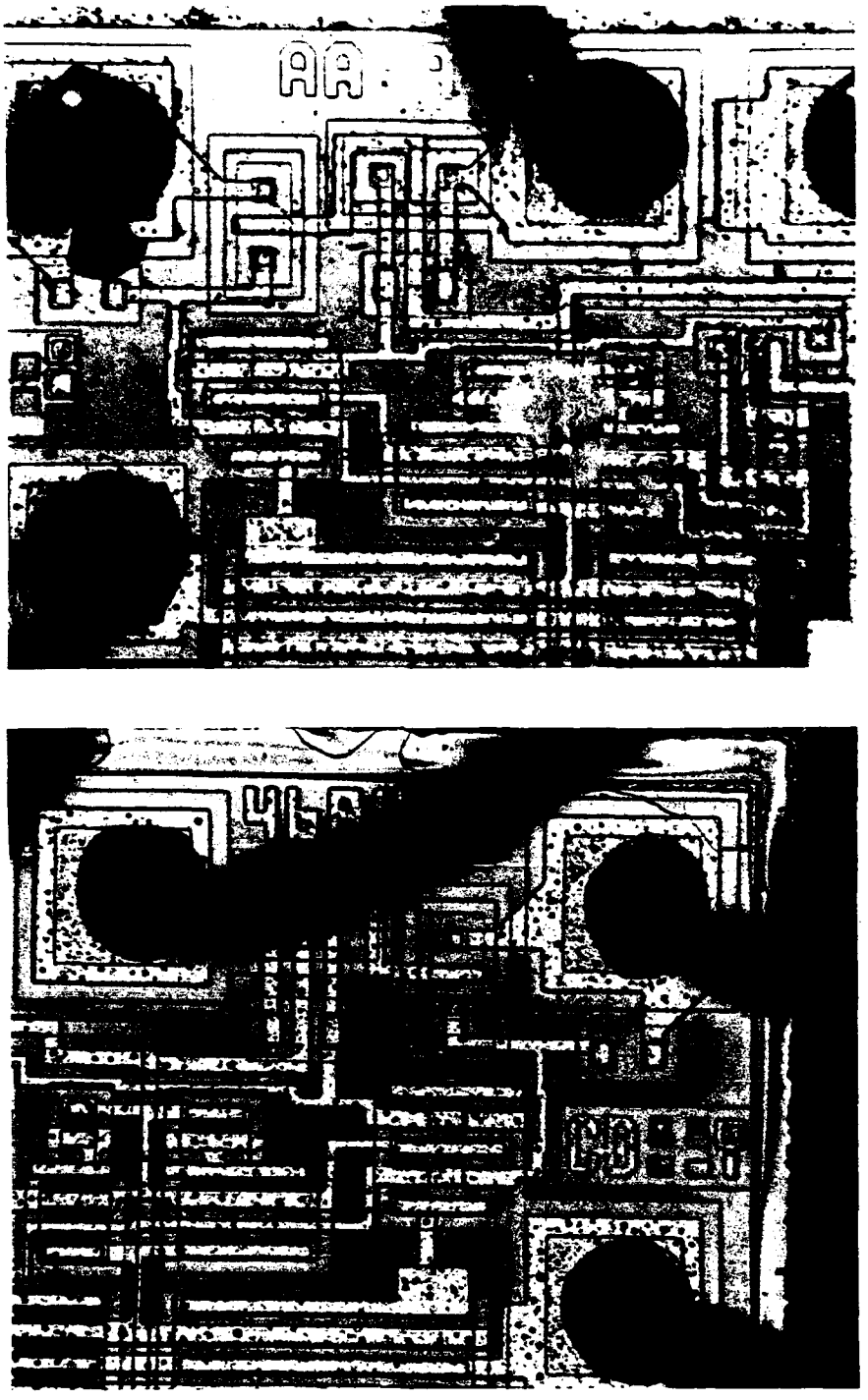


Figure 34. Comparison of the bond pad appearance after 1000 hours of sequential autoclave exposure between a standard die and a ceramic-coated die (PDIPs) 100X.

Sequential Temperature Cycling with Salt Fog Exposure

After a total of 1000 cycles (hours) of sequential temperature cycling, the devices were subsequently subjected to 24 hours of salt fog exposure. The reliability results from the sequential test exposure (Sequence B) are shown in Figure 35. Although the plasma-SiC coating extended out onto the leadframe surface, a high integrity seal was maintained where the leadframe external pins exit the EMC even after 1000 temperature cycles.

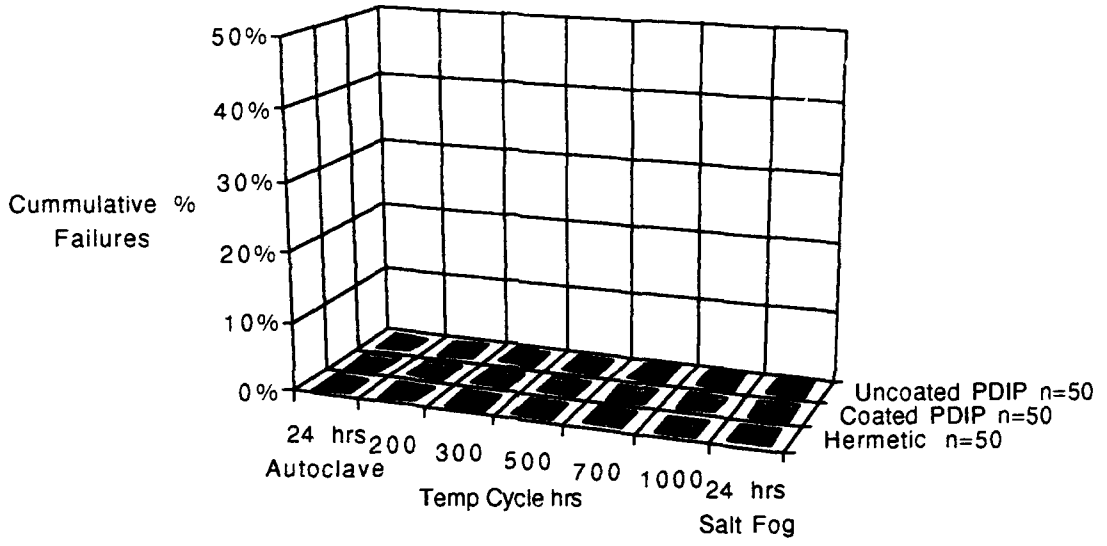


Figure 35. Reliability data of CD4011B devices from sequential temp cycle with salt fog exposure.

HAST Exposure

Since HAST exposure clearly differentiated the level of reliability provided by each packaging system, detailed information regarding this test is included to better understand the accelerated failure mechanisms.

HAST exposure at 159°C approaches the glass transition temperature (T_g) of the EMC, which is approximately 165°C. Although this test condition does not represent real field service conditions, this exposure will force any ionic impurities from the EMC to the die surface. This presented a unique opportunity to thoroughly assess the ion and moisture barrier properties of the ceramic coatings. Much of Dow

Corning's previous HAST data was obtained at 159°C, which, for correlation purposes, allowed their use as baseline information on the CD4011B [4,8,15].

HAST exposure was accomplished by randomly assembling all device configurations onto stitch bonded polyimide boards. The devices were biased when the chamber equilibrated at set point conditions and not during ramp-up or ramp-down periods. The device was normally biased with outputs floating and 10 volts dc bias on alternating inputs which is shown in Figure 36. This biasing scheme permitted the device to be turned on with minimal current flow (quiescent current <4 μA), reducing or minimizing the junction temperature to insure retention of the ambient humidity at the device surface.

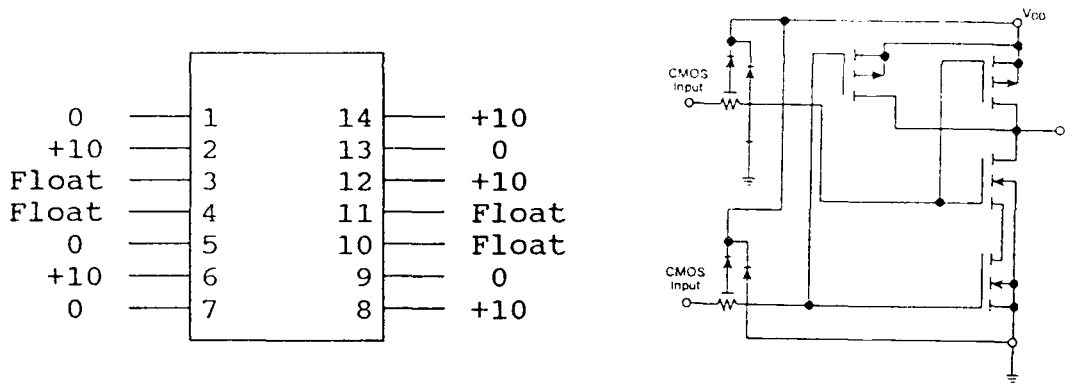


Figure 36. HAST Biasing Scheme for CD4011B CMOS Quad Dual Input NAND Gate Device.

Failure Analysis of Plastic and Hermetic Packaged CMOS Devices

Analysis of the potential failures subjected to direct and sequential HAST exposures was performed by Oneida Research Services. This failure analysis was conducted to identify the physical degradation mechanisms which led to device failure in HAST and to determine any differences in failure mode between ceramic-coated die or standard die in plastic and hermetic packages. A further objective was to examine ceramic-coated die which survived 1000 hours of HAST exposure to gain further understanding of the phenomena unique to this thin-film packaging technology which can lead to device failure.

A total of eighteen representative devices consisting of standard PDIPs, coated PDIPs, and hermetic controls which failed HAST exposure were randomly selected within specific time intervals for failure analysis. Four additional coated PDIPs which were still functional after 1000 hours were randomly selected and submitted for analysis. Internal water vapor (IWV) analysis was performed on the hermetic control devices prior to submission for failure analysis. Full electrical (parametric) test data was submitted for each device and electrical failures were confirmed on representative samples by dc parametric curve tracing. Table 4 lists the basic characteristics of the 22 devices selected for failure analysis.

Table 4. CMOS devices selected for failure analysis

Seq	Device Type	S/N	HAST hrs	Electrical Test	Decap Method	Verified Corrosion Failure
A	Standard	031	300	Fail	Liquid	Y
A	Standard	027	600	Fail	Liquid	Y
A	Standard	042	800	Fail	Liquid	Y
A	Ceramic-coated	033	600	Fail	Liquid	N
A	Ceramic-coated	034	1000	Fail	Liquid	Y
A	Ceramic-coated	040	1000	Good	Liquid	-
A	Ceramic-coated	041	1000	Good	Mechanical	-
A	Hermetic	036	1000	Fail	Mechanical	N
A	Hermetic	047	1000	Fail	Mechanical	N
B	Standard	133	200	Fail	Liquid	N
B	Standard	119	400	Fail	Liquid	Y
B	Standard	138	500	Fail	Liquid	Y
B	Standard	110	600	Fail	Liquid	Y
B	Ceramic-coated	112	400	Fail	Liquid	Y
B	Ceramic-coated	146	600	Fail	Liquid	Y
B	Ceramic-coated	137	800	Fail	Liquid	N
B	Ceramic-coated	103	1000	Fail	Liquid	Y
B	Ceramic-coated	135	1000	Fail	Mechanical	Y
B	Ceramic-coated	140	1000	Good	Liquid	-
B	Ceramic-coated	141	1000	Good	Mechanical	-
B	Hermetic	145	800	Fail	Mechanical	N
B	Hermetic	146	900	Fail	Mechanical	N

External Appearance

Initially all submitted devices were examined by stereoscopic microscopy for overall external appearance, package markings, and the sealing of the leads. Devices subjected to sequential HAST exposure (sequence B) showed slightly more corrosion on the leads and corrosion byproducts between the leads than those subjected to direct HAST exposure (sequence A). However, the level of corrosion is at a level typical for the HAST exposure. There were no other changes in the appearance of the devices.

Radiography

Radiographs were then made of nine representative devices (7 - standard PDIPs and 2 - ceramic-coated PDIPs), in accordance with MIL-STD-883 Method 2012. All devices displayed poor wire sweep (e.g. wires that deviate from the straight line between bond pad and leadframe). There was no difference in the wire sweep between standard and coated PDIPs. No other anomalies, such as extraneous material, excess or voided bonding material were observed.

Internal Water Vapor

Internal water vapor tests were conducted on the hermetic devices by Atlantic Analytical Laboratory. These results are shown in Tables 5 & 6. Sequence A devices S/N 032 and 036 displayed excessively high moisture and hydrogen levels. Although failed device S/N 036 displayed the most severe physical degradation, and highest moisture content there appears to be no direct correlation between moisture content and device failure.

Table 5. Internal Water Vapor of Hermetic Packaged CMOS Devices (Sequence A)

CD4011B	Sequence	A	A	A	A	A	A
	Unit No.	27	32	36	40	45	47
Amt of Gas	cc	0.019	0.073	0.051	0.019	0.019	0.019
Nitrogen	%	99	37	39	99	99	99
Oxygen	ppm	ND	ND	ND	ND	ND	ND
Argon	ppm	230	120	110	280	240	210
Carbon Dioxide	ppm	590	800	580	390	500	490
Moisture	ppm	400	218000	224000	420	950	680
Hydrogen	ppm	ND	407000	377000	ND	ND	ND
Helium	ppm	ND	ND	ND	ND	ND	ND
Fluorocarbons	ppm	ND	ND	ND	ND	ND	ND
Organics	ppm	ND	ND	ND	ND	ND	ND

Table 6. Internal Water Vapor of Hermetic Packaged CMOS Devices (Sequence B)

CD4011B	Sequence Unit No.	B 103	B 108	B 119	B 130	B 145	B 146
Amt of Gas	cc	0.019	0.019	0.018	0.019	0.019	0.019
Nitrogen	%	99	99	99	99	99	99
Oxygen	ppm	ND	ND	ND	ND	ND	ND
Argon	ppm	290	260	170	230	350	330
Carbon Dioxide	ppm	380	370	360	440	730	370
Moisture	ppm	1440	930	1000	1500	690	1240
Hydrogen	ppm	ND	ND	ND	ND	ND	ND
Helium	ppm	ND	ND	ND	ND	ND	ND
Fluorocarbons	ppm	ND	ND	ND	ND	ND	ND
Organics	ppm	ND	ND	ND	ND	ND	ND

Internal Inspection

Most PDIPs were liquid decapsulated using red fuming nitric acid in a Nippon Scientific PA102 Plastic Mold Decapsulation system. For this liquid decapsulation process, the device is exposed to the very anhydrous nitric acid at a temperature of 65°C for 2 to 4 minutes. Recognizing that the liquid decapsulation process might damage some features to be observed on the die of the PDIPs, three coated PDIPs were also mechanically decapsulated. Mechanical decapsulation of PDIPs was performed by heating the packages on a hot plate and breaking the EMC away from the die with small fine cutting diagonal pliers. The hermetic devices were decapsulated mechanically using an Exacto™ knife.

The die of all devices were inspected by optical microscopy, typically at 20 to 250X magnification and photomicrographs were made of pertinent features. Several devices were also analyzed by scanning electron microscopy and energy dispersive X-ray microanalysis (EDS) for specific elemental information. These observations were then compared with the parametric test data (57 parameters) for each device.

Failure Analysis Results

1. Standard die in plastic packages (standard PDIPs) displayed classical anodic corrosion of the biased aluminum bond pads which is shown in Figure 37; this caused open circuit failures of the CMOS devices. The corrosion was confirmed to be due to both dissolution of aluminum and migration of halide ions [16-19].

2. Most failures of the experimental ceramic-coated die in plastic packages (coated PDIPs) seem to be from non-classical corrosion mechanisms, prior to 800 hours of HAST. The failed coated PDIPs primarily displayed catastrophic dissolution of all aluminum bond pads with, for some die, complete dissolution of ground and output circuit traces. Other failure mechanisms of the coated PDIPs included classical anodic corrosion of only the floating output aluminum bond pads [16-19], anodic dissolution of gold ball bonds [16,19], and electrical overstress [20,21]. Figure 38 depicts bond pad corrosion of the floating outputs. It is not clearly understood why only the floating output bond pads showed signs of corrosion and not the biased terminals. Figures 39 and 40 depict anodic dissolution of gold ball bonds and electrical overstress.

   Classical anodic corrosion of aluminum at the biased pads was the predominant failure mechanism for failure beyond 800 hours of HAST, possibly due to coating defects and/or diffusion related mechanisms. Functional ceramic-coated die after 1000 hours of sequential HAST show initial signs of classical anodic corrosion of biased aluminum bond pads. Figure 41 compares the die condition of both standard and ceramic-coated PDIPs.

3. The hermetic control device failures were due to anodic dissolution/migration of aluminum at biased bond pad fillet regions [16-19], aluminum-silicon alloying at the input diode junctions [21,22] and electrical current overstress [20,21], that resulted in open and short circuits, as shown in Figure 42.

4. Although the preconditioning of the devices prior to HAST exposure (sequential HAST) significantly increased the failure rate of the standard DIPs, no evidence was obtained that suggests a change in the failure mode. There was minimal change in failure rate and no change in failure mode observed on the ceramic-coated PDIPs or the hermetic controls as a result of sequential HAST.

5. For some standard (uncoated) and ceramic-coated die, metallic silver flakes from the die attach were deposited on the gold wires, from the span to the bond pad. These flakes were observed on the preconditioned devices after 600 hours of HAST exposure for the standard die and after 800 hours for the ceramic-coated die. An additional 200 hours of HAST exposure were required for these silver flakes to be seen on devices which were not preconditioned.

6. No device failures were determined to be due to contamination from assembly (die attach and wirebond), handling, or from the inorganic coating materials and processes.

7. The application of the ceramic coatings at 250°C did not affect wirebond interconnections or alter the leadwire sweep. It did not appear that the ceramic coatings were adversely affected by the molding process.

8. Standard failure analysis techniques could be used to decapsulate plastic packages with the ceramic coatings (both liquid and mechanical) and assess the device failure modes.

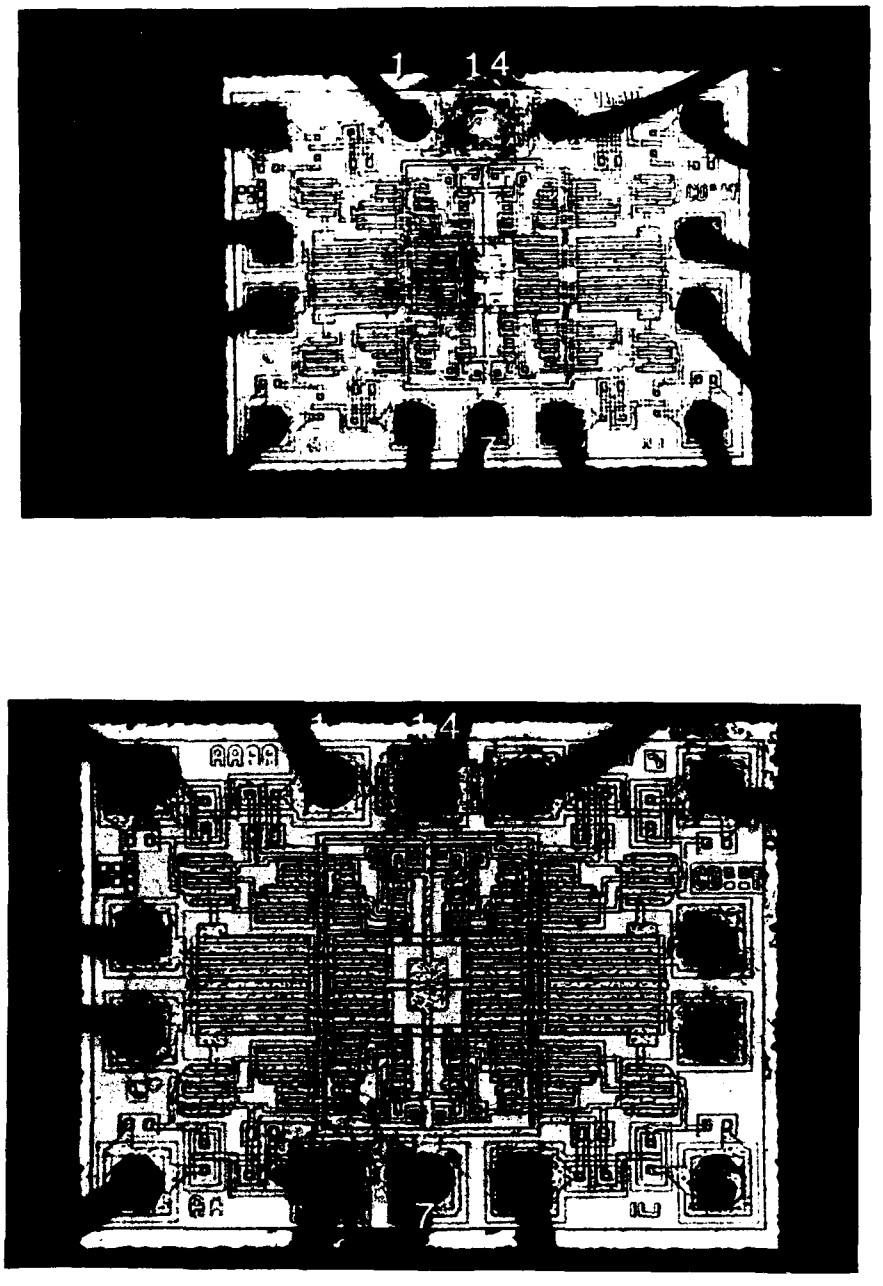
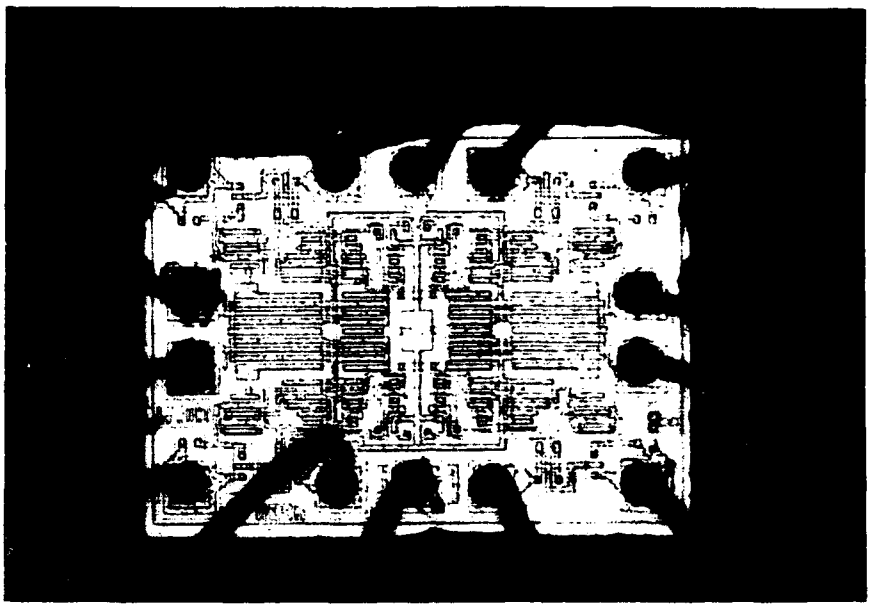


Figure 37. Failure analysis of standard die in plastic package reveals severe bond pad corrosion. (s/n 119 & 027 after 400/600 hours sequential HAST exposure).



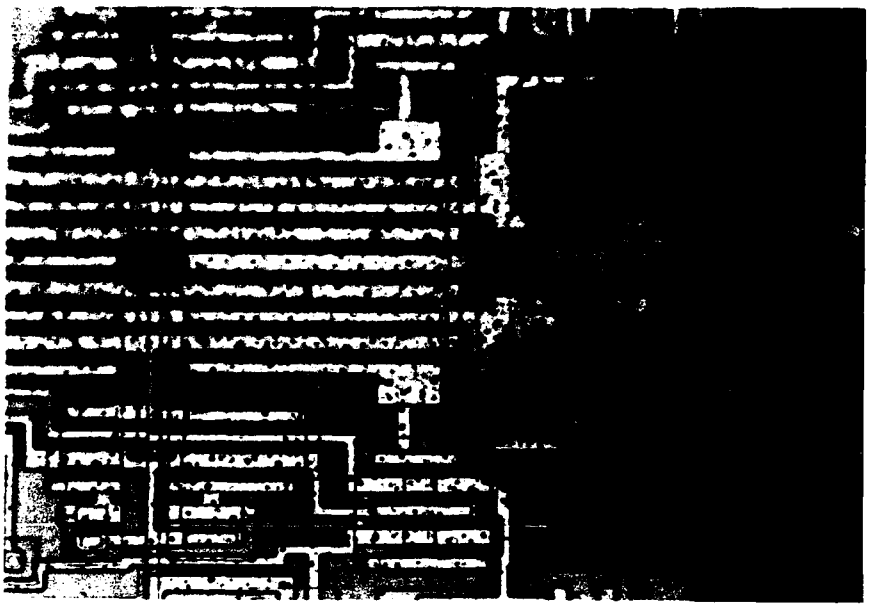


Figure 38. Failure analysis of ceramic-coated die in plastic package reveals bond pad corrosion. (s/n 146 after 600 hours sequential HAST exposure).

Figure 39. Failure analysis of ceramic-coated die in plastic package reveals anodic dissolution of gold ball bonds and current overstress. (s/n 034 after 1000 hours sequential HAST exposure).

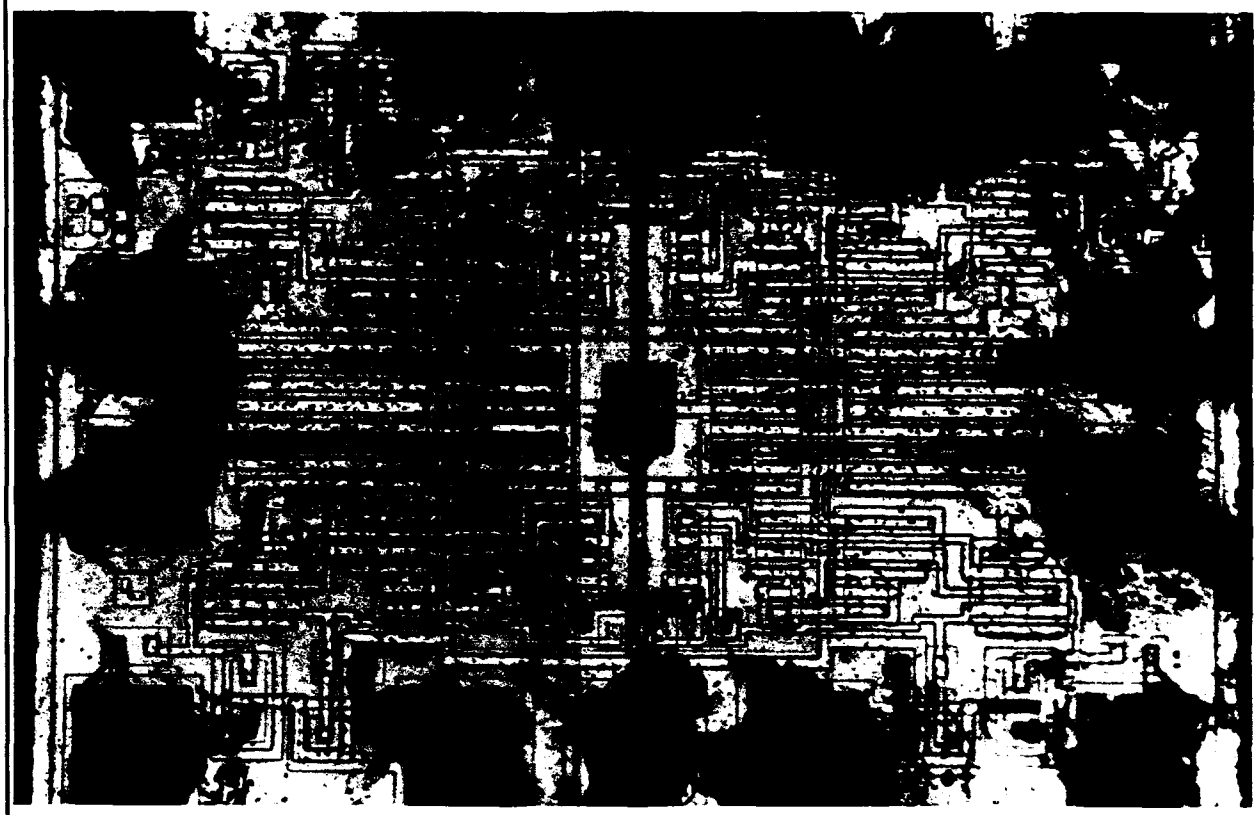
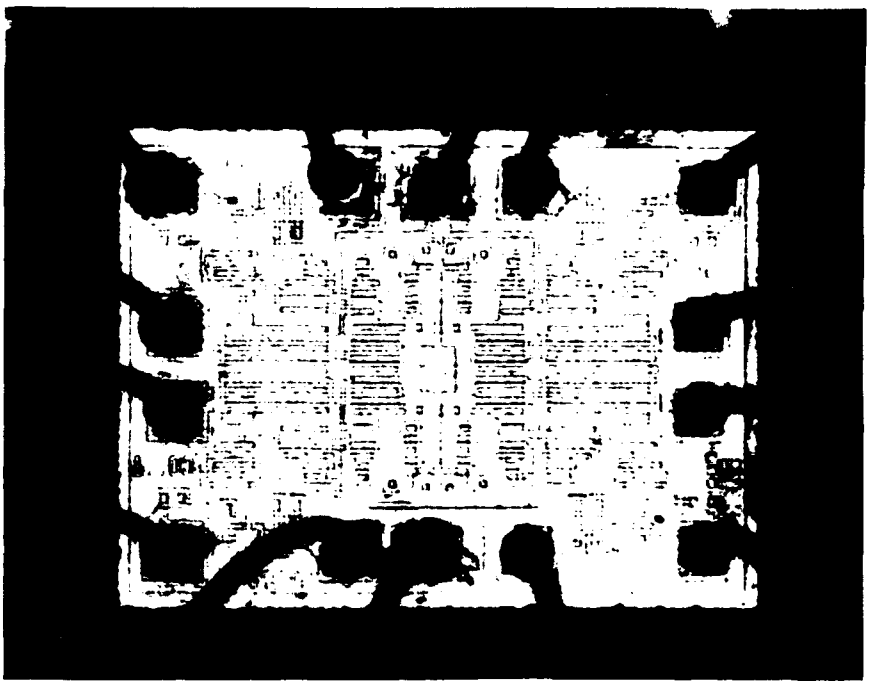


Figure 40. Failure analysis of ceramic-coated die in plastic package reveals anodic dissolution of gold ball bonds and current overstress. (s/n 034 after 1000 hours sequential HAST exposure).



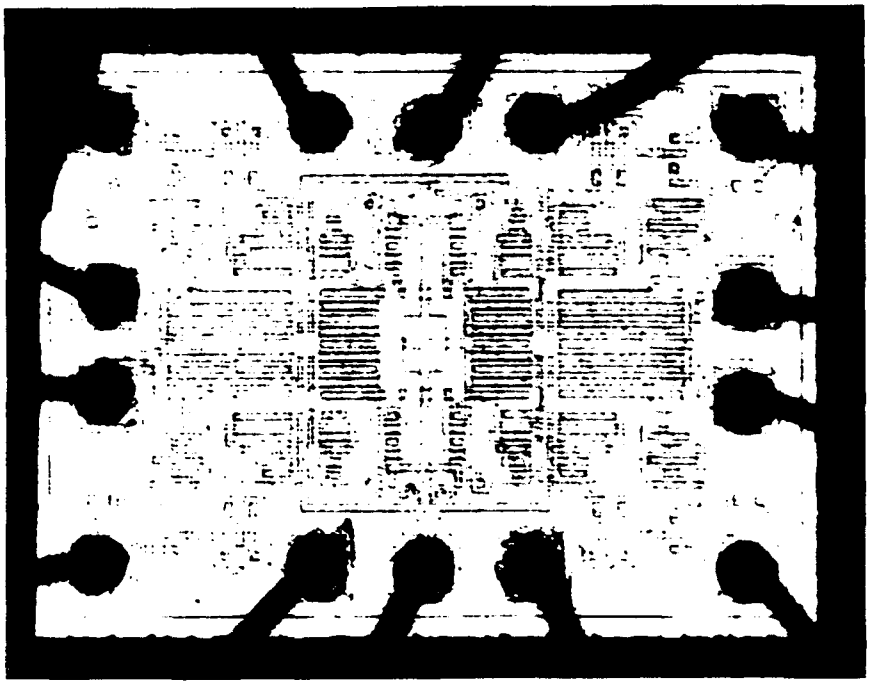


Figure 41. Comparison of standard commercial (top) and ceramic-coated (botom) die at 500 and 1000 hours respectively.

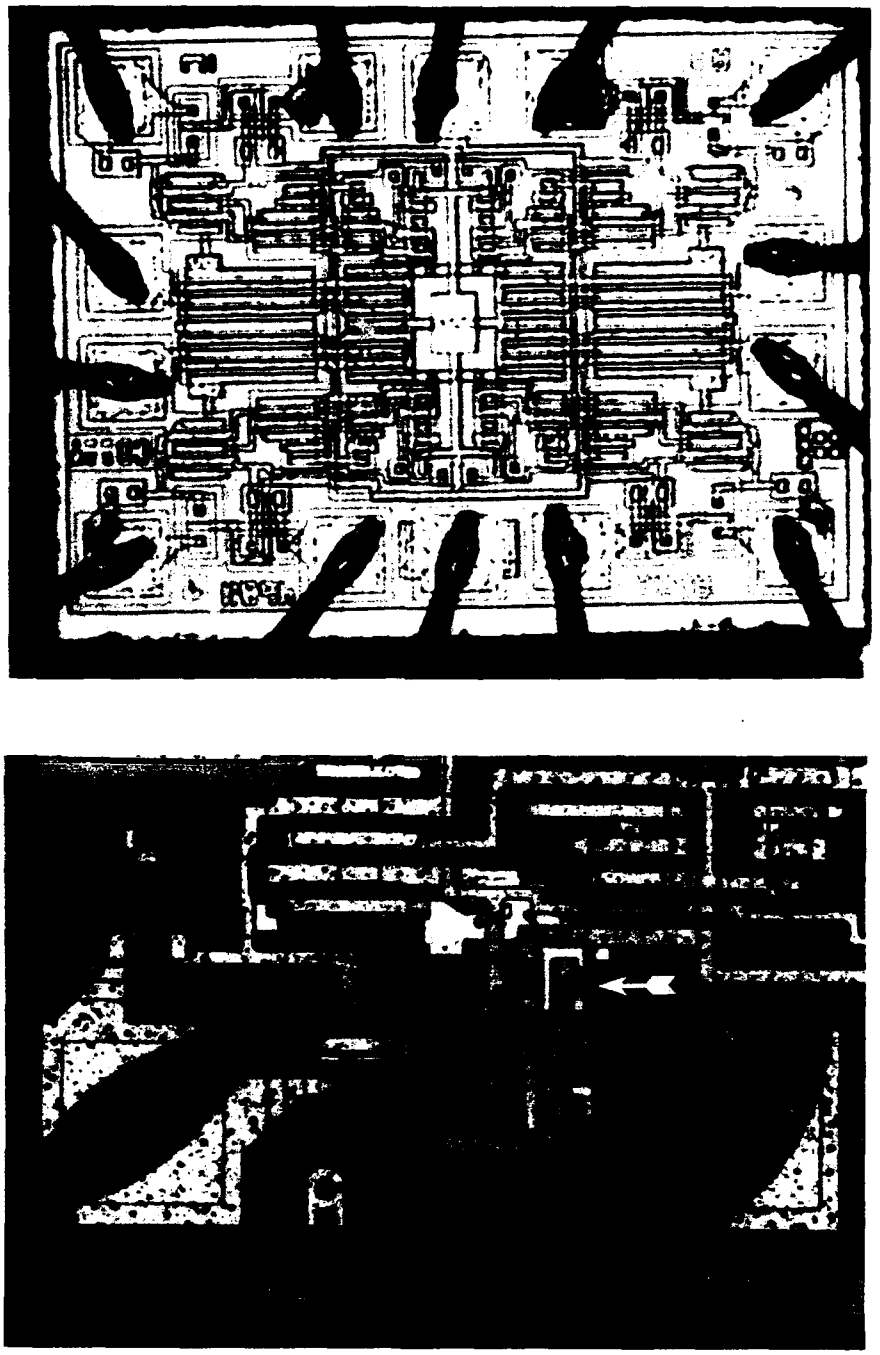


Figure 42. Failure analysis of standard die in hermetic package reveal electrical current overstress. (s/n 036 after 1000 hours sequential HAST exposure).

Reliability results after failure analysis from direct HAST exposure (Sequence A) are shown in Table 7; sequential HAST exposure (Sequence B) are shown in Table 8. The HAST data clearly indicates that the reliability of coated PDIPs far surpasses the reliability of standard PDIPs; coated PDIPs closely approach the reliability of traditional hermetic packaging. Failures of standard PDIPs reached 50% after approximately 500 hours of sequential HAST and reached 90% failure at 700 hours. Sequential testing of plastic package devices increased the failure rate of standard PDIPs but had little to no affect on coated PDIPs. Figures 43 and 44 show graphical representations of Table 7 and Table 8 respectively.

Table 7. Reliability Data of CD4011B Devices in HAST (n=25)

Sequence A: hours>	100	200	300	400	500	600	700	800	900	1000
Hermetic Controls	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/25	0/24	0/24
Standard PDIPs	0/25	0/25	1/25	1/25	4/25	10/25	15/25	19/25	23/25	24/25
Ceramic-coated PDIPs	0/25	0/25	0/25	0/25	0/25	0/25	0/23	0/23	2/23	4/23

Table 8. Reliability Data of CD4011B Devices in Sequential HAST Exposure (n=50)

Sequence B: hours>	100	200	300	400	500	600	700	800	900	1000
Hermetic Controls	0/50	0/50	0/50	0/50	0/50	0/50	0/50	0/50	0/48	0/47
Standard PDIPs	0/50	0/50	3/48	7/48	20/48	38/48	43/48	46/48	48/48	48/48
Ceramic-coated PDIPs	0/50	0/50	0/50	0/50	0/50	3/49	3/49	3/49	7/45	13/45

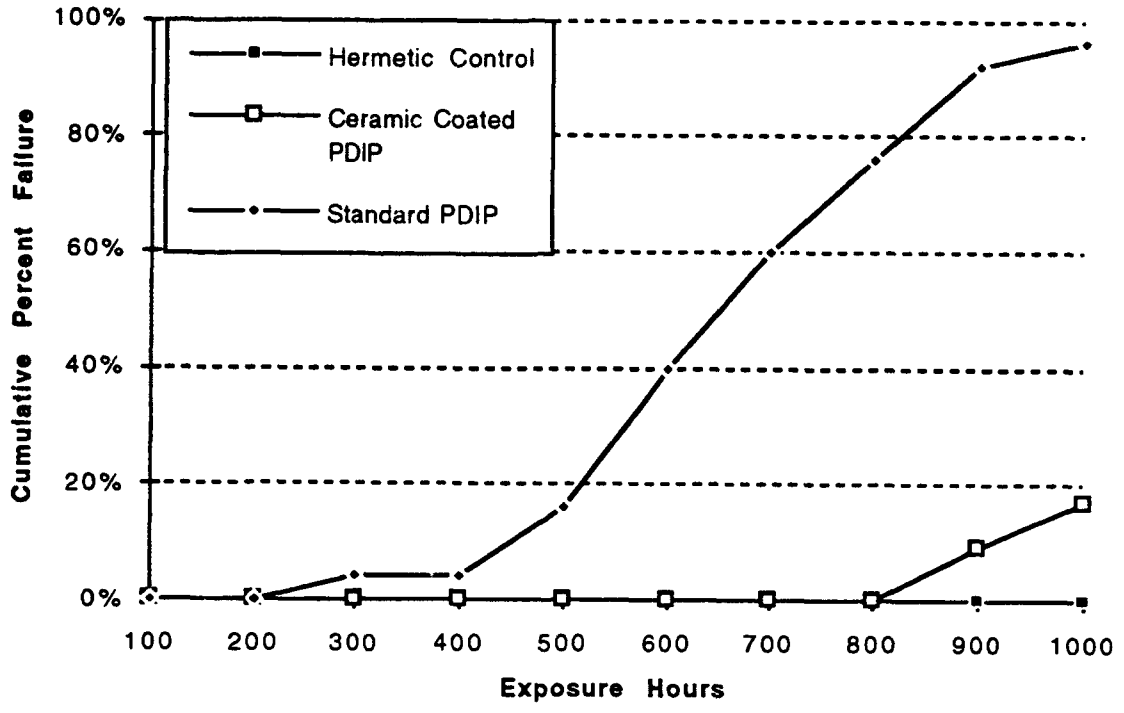


Figure 43. Graphical Representation of Reliability Data for CD4011B Devices in Direct HAST Exposure.

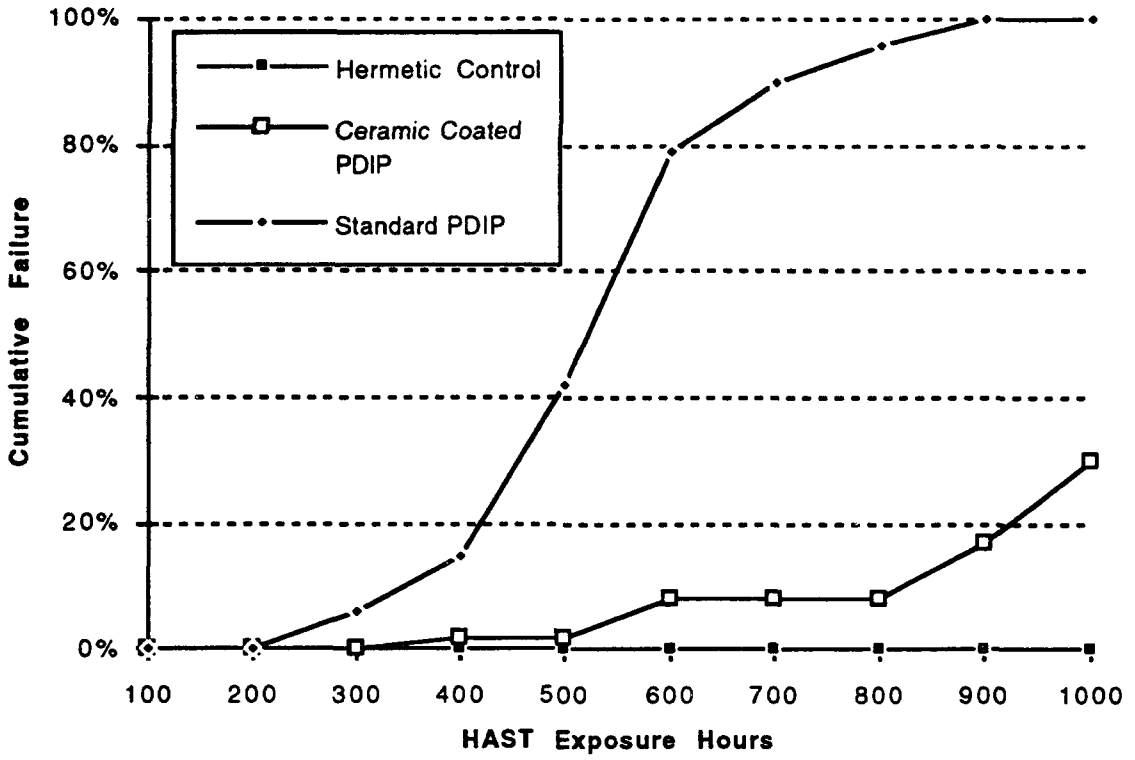


Figure 44. Graphical Representation of Reliability Data for CD4011B Devices in Sequential HAST Exposure.

An analysis of randomly selected functional CMOS devices exposed to 1000 hours of sequential HAST revealed that both coated PDIPs and hermetic package controls exhibited minor bond pad corrosion at biased (V^+) inputs. No standard PDIPs survived 1000 hours of sequential HAST.

The application of the inorganic coatings did not adversely effect the electrical performance of the integrated circuit even after 1000 hours of sequential reliability testing. The data suggests that the preconditioning exposure used in sequential testing accelerated device degradation with no change in failure mode. The data also suggests that the inorganic coatings are compatible with present state-of-the-art semiconductor passivation materials (>400°C) and backend assembly processes.

Parametric Shift Analysis

As described earlier in this report, full electrical (parametric) testing was performed on each CMOS device at specified environmental exposure intervals. The serialization of the devices permitted an opportunity to assess any change in electrical characteristics (parametric shift) during the environmental exposure. Since device failures resulted from each configuration under HAST exposure, this parametric data was analyzed to provide comparative results for both shifts leading to device failure within a configuration and those shifts between different configurations.

Parametric shift analysis of all CD4011B CMOS devices subjected to HAST exposure was completed for the standard PDIPs, ceramic coated PDIPs and hermetic control devices. The parameters analyzed included input current, output current, quiescent current, and voltage output at both 5 and 15 volts. The most sensitive parameter for shift analysis appeared to be the input current measurements (pins 1,2,5,6,8,9,12,13). The rest of the parametric data generally shows significant results only after catastrophic failure of the device.

There are significant differences among the results from the three device configurations. Figure 45 shows the parametric shift results of a representative sampling from each configuration. The worst scatter and increasing average values of input current occur with the standard PDIP units. A significant shift starts around 300 hours in HAST and failures start occurring in great numbers around 500 hours. These shifts seem to stabilize at an increased level but below the failure limit until the device fails.

The ceramic coated PDIP devices start showing some shift activity in the 600 hour region with an occasional failure while the hermetic devices start showing activity in the 600 - 800 hour region also with an occasional failure. The hermetic package is the least active of the devices with regard to parametric shifts.

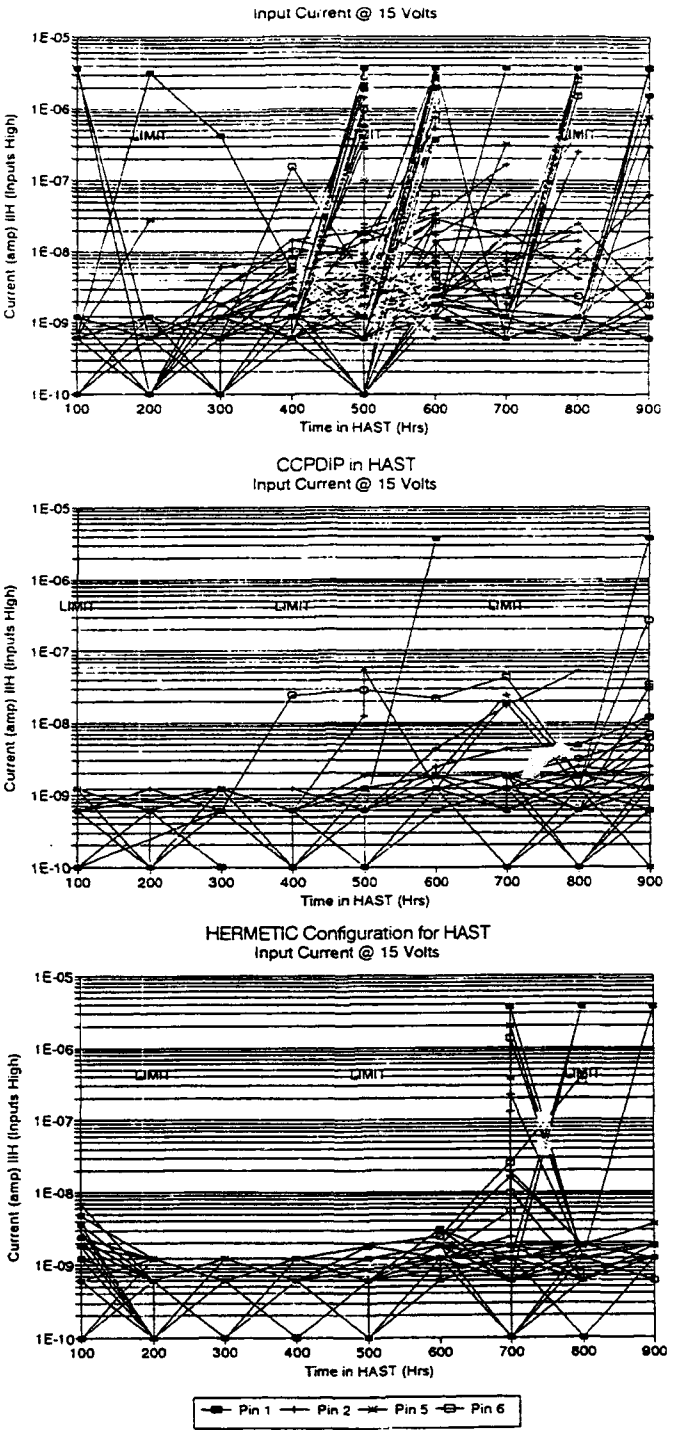


Figure 45. Parametric shift analysis results for three device packaging configurations.

The parametric shift analysis had good correlation with the HAST reliability data. No difference in parametric shift was found between devices subjected to direct or sequential testing other than a 100 hour decrease in the time the shifts started (standard PDIPs). Good correlation of the parametric data was also found with Weibull analysis, which is subsequently described in this report.

Weibull Analysis

The reliability data generated in this study on CMOS devices demonstrated the improved device reliability provided by a low temperature ceramic coating technology. Beyond that, the failure rates calculated from the HAST data may be used to predict the comparative component lifetime. Although failure modes were significantly different between standard and coated PDIPs, an attempt was made to assess the data using a conventional model. It should be clearly understood that this evaluation is a worst case scenario for the ceramic coated PDIPs since it assumes that all of these failures were due to bond pad corrosion. The failure modes were actually assessed on a random sampling of failed devices by Oneida Research Services and found to include catastrophic dissolution of all aluminum bond pads with output and ground surface metallizations, electrical current overstress, gold anodic dissolution, and silicon-aluminum interdiffusion at input diodes. Conventional bond pad corrosion was observed in exposures greater than 800 hours. Detailed failure analysis may be found earlier in this report (page 76).

For comparison of results, the failure rates for the test configurations were calculated from the ratio (# of failures) / (cumulative device test time). From the test data, obtained at a temperature of 159°C, the comparative long term storage lifetime can be calculated assuming a thermally activated failure mechanism (for bond pad corrosion) following an Arrhenius expression (Lawson Model). For this mode, an activation energy of 0.7 eV has been suggested [23]. This gives an acceleration factor for storage at 30°C of 2,978. As shown in Tables 9 and 10, the instantaneous failure rate of standard PDIPs at 600 hours of HAST is more than 1 order of magnitude greater than for coated PDIPs. Six hundred hours of HAST exposure is approximately the mean-time-to-failure of standard PDIPs in both direct and sequential testing.

Table 9. Evaluation of HAST Reliability Data by Weibull Analysis (Sequence A)

Test Configuration	Time to First Failure	MTTF (hrs)	Failure Rate at 600 hr (per thousand)	Failure Rate at 30°C (FIT)
Standard PDIP	300	676	2.70	455
Coated PDIPs	900	1192	0.059	59

Table 10. Evaluation of Sequential HAST Reliability Data by Weibull Analysis (Sequence B)

Test Configuration	Time to First Failure	MTTF (hrs)	Failure Rate at 600 hr (per thousand)	Failure Rate at 30°C (FIT)
Standard PDIP	300	544	6.55	586
Coated PDIPs	600	1392	0.308	100

The Weibull statistics clearly indicates that the reliability of state-of-the-art commercial plastic encapsulated devices can be improved by at least one order of magnitude when the die are coated with thin-film ceramic coatings prior to epoxy overmolding. Although this is a worst case evaluation since only a sampling of the failed ceramic coated devices were submitted for failure analysis, it does provide a good opportunity to use conventional models for understanding the reliability data generated in this study.

Ceramic Open Cavity CMOS Devices

The reliability of bare CMOS devices in ceramic chip carriers was assessed for correlation for possible future MCM application. These bare die, assembled in open cavity sidebrazed packages (D-packages), were subjected to all of the environmental stress exposures without a lid.

A random sampling of both standard and ceramic-coated die in D-packages, which were still fully functional during the reliability testing intervals, were visually inspected for signs of aluminum bond pad degradation. This data is included throughout the reliability testing to identify when the aluminum metallization begins to degrade leading to failure.

Preconditioning Exposure

Significant performance differentiation between standard and ceramic-coated die was obtained after preconditioning exposure. A total of 15.5% of standard D-packages and 0.3% of coated D-packages failed from the preconditioning exposure.

Failure analysis of standard and ceramic-coated D-packages clearly provided the basis for understanding the difference in device performance. Standard D-packages displayed severe aluminum leadwire corrosion (swollen wires). Additionally, analysis of randomly selected functional standard D-packages revealed the same degree of severe leadwire and some ongoing bond pad corrosion.

A coated D-package displayed an isolated leadwire corrosion at the neckdown to frame post region (outer-lead bond. OLB). The remainder of the device appears good, with no visible signs of leadwire or bondpad corrosion. Analysis of randomly selected functional coated D-packages revealed no visible signs of leadwire or bondpad corrosion. Visual inspection of both the coated and uncoated D-packages subsequent to autoclave exposure revealed that all of the devices were completely covered with a transparent foreign film. This foreign film may affect the failure mode of the standard die in long term environmental exposures.

Autoclave Exposure

Reliability test results from direct and sequential autoclave exposures are shown in Figures 46 and 47 respectively. The autoclave data clearly indicates that the

reliability of coated D-packages far exceeds that of standard D-packages. Differentiation between standard and coated D-packages was achieved after 100 hours of autoclave exposure. A significant improvement in moisture protection (autoclave) was obtained using the ceramic coatings.

The comparative data illustrated between Figures 46 and 47 suggests that the preconditioning exposure accelerated the hazard rate of early failures in autoclave. Failure analysis of standard and coated D-packages revealed very specific failure modes which corresponded with the device electrical data. No difference in failure mode was observed between direct or sequential autoclave exposures. Standard D-packages failed by multiple open circuits caused by severe aluminum leadwire corrosion, as shown in Figure 48. Longer autoclave exposures also revealed signs of bond pad corrosion. Device inspections as early as 100 hours into test revealed that all of the D-package devices were completely covered with a transparent foreign film, as shown in Figure 49. The source of the transparent foreign film was not found. Prior work by DCC has shown that device failures due to bondpad corrosion occurs at <100 hours autoclave exposure for standard D-packages [24]. The foreign film observed on the die would account for the increased lifetime of the device before bond pad corrosion was found. Coated D-packages failed by single open circuits caused by isolated aluminum leadwire corrosion at the OLB on the package, as shown in Figure 50. No chip related failures were observed on coated D-packages. It should be no surprise that ceramic-coated leadwires unprotected from mechanical shock and vibration will fracture the coating at high stress regions, namely the bondpad and framepost regions.

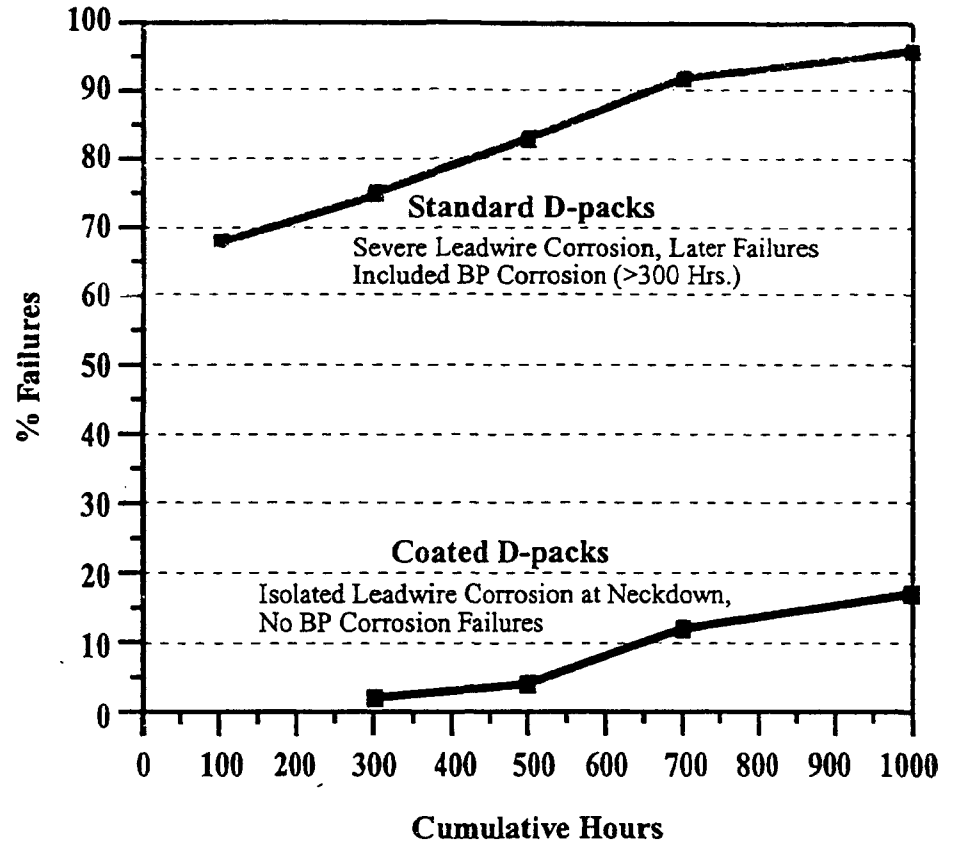


Figure 46. Graphic illustration of the performance data on CD4011B CMOS devices in autoclave testing.

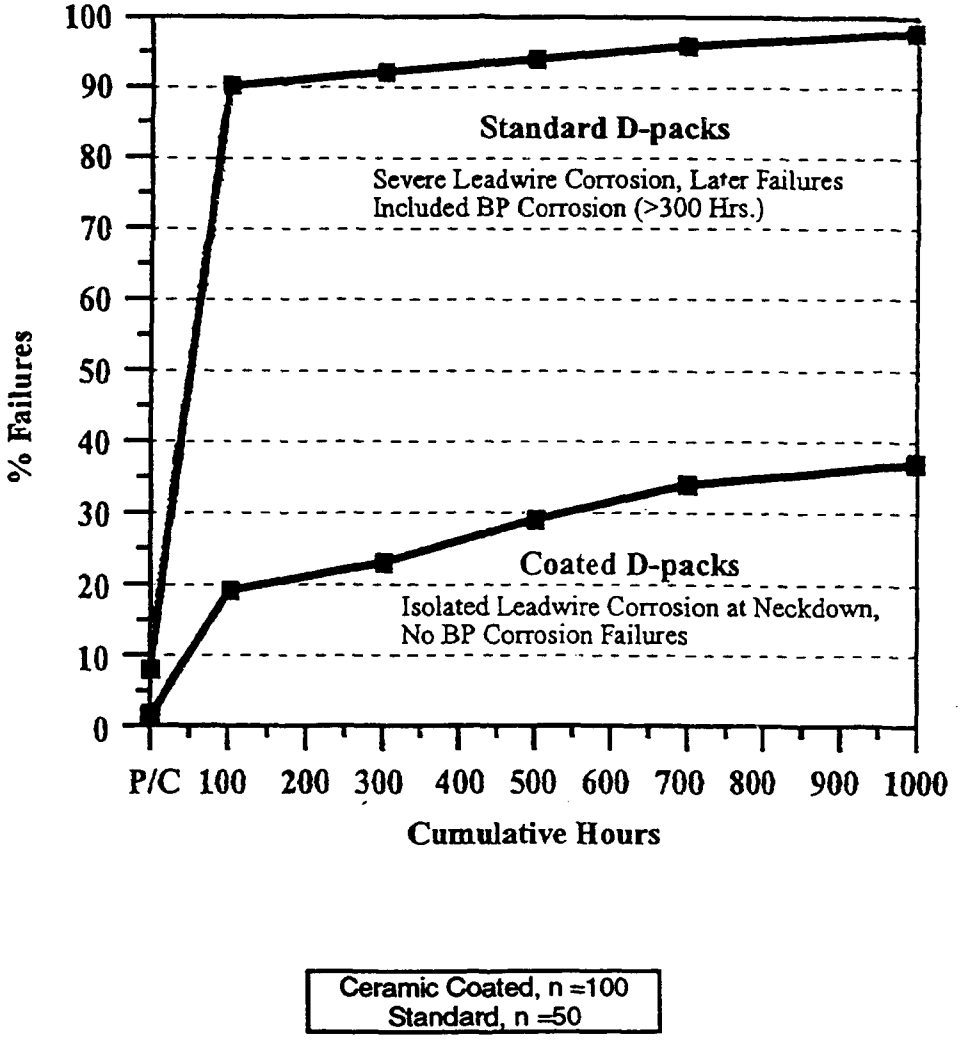
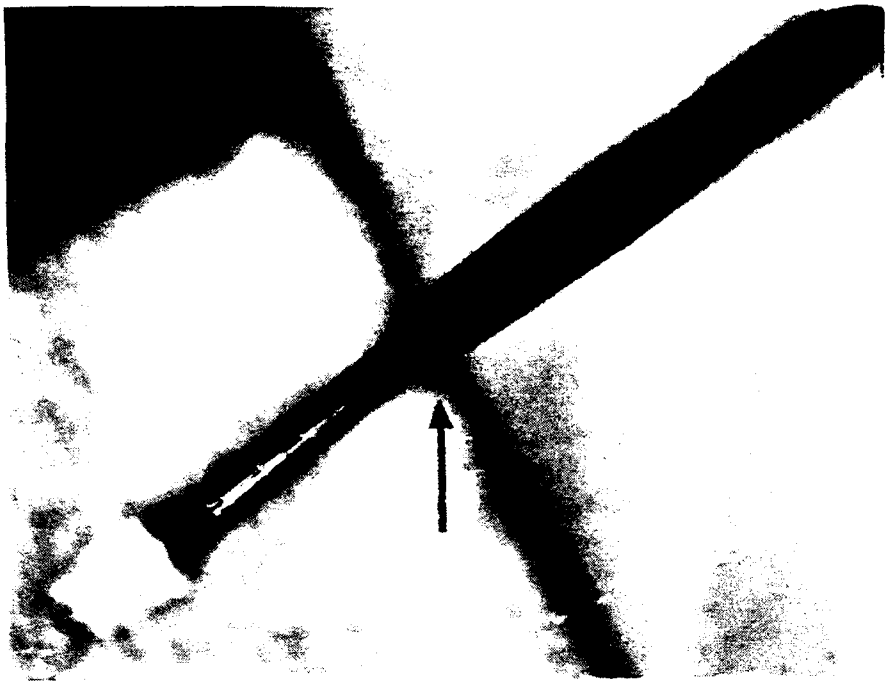


Figure 47. Graphic illustration of the performance data on CD4011B CMOS devices in sequential autoclave testing.



(a) s/n 002 (200X).

(b) s/n 002 (100X)

Figure 48. Swollen aluminum leadwires resulting from severe corrosion after 100 hrs of autoclave exposure of a standard D-package.

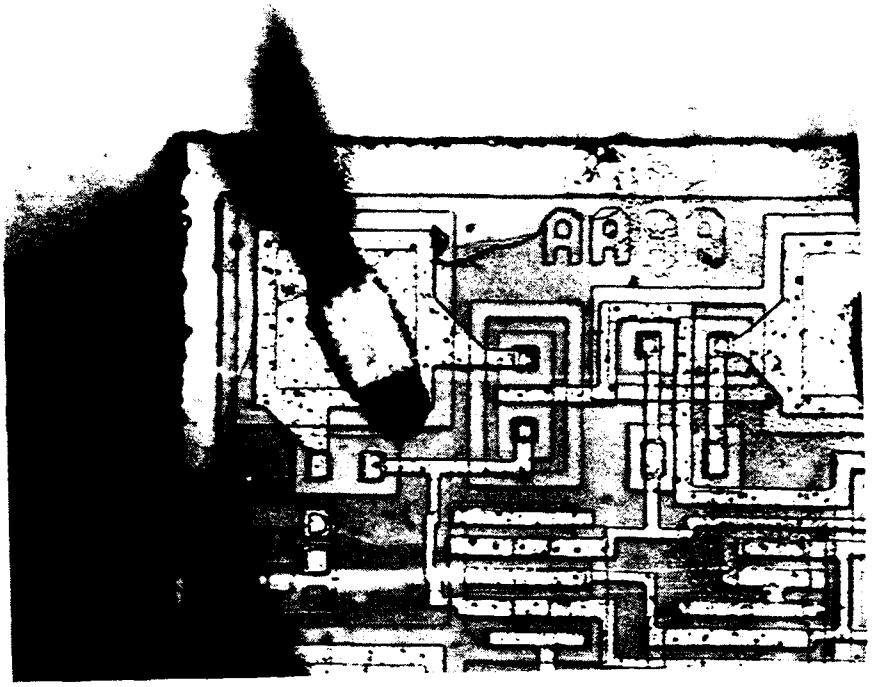


Figure 49. Close-up view of die showing deposit of foreign film on the die from autoclave exposure of a standard D-package, s/n 074. (200X)

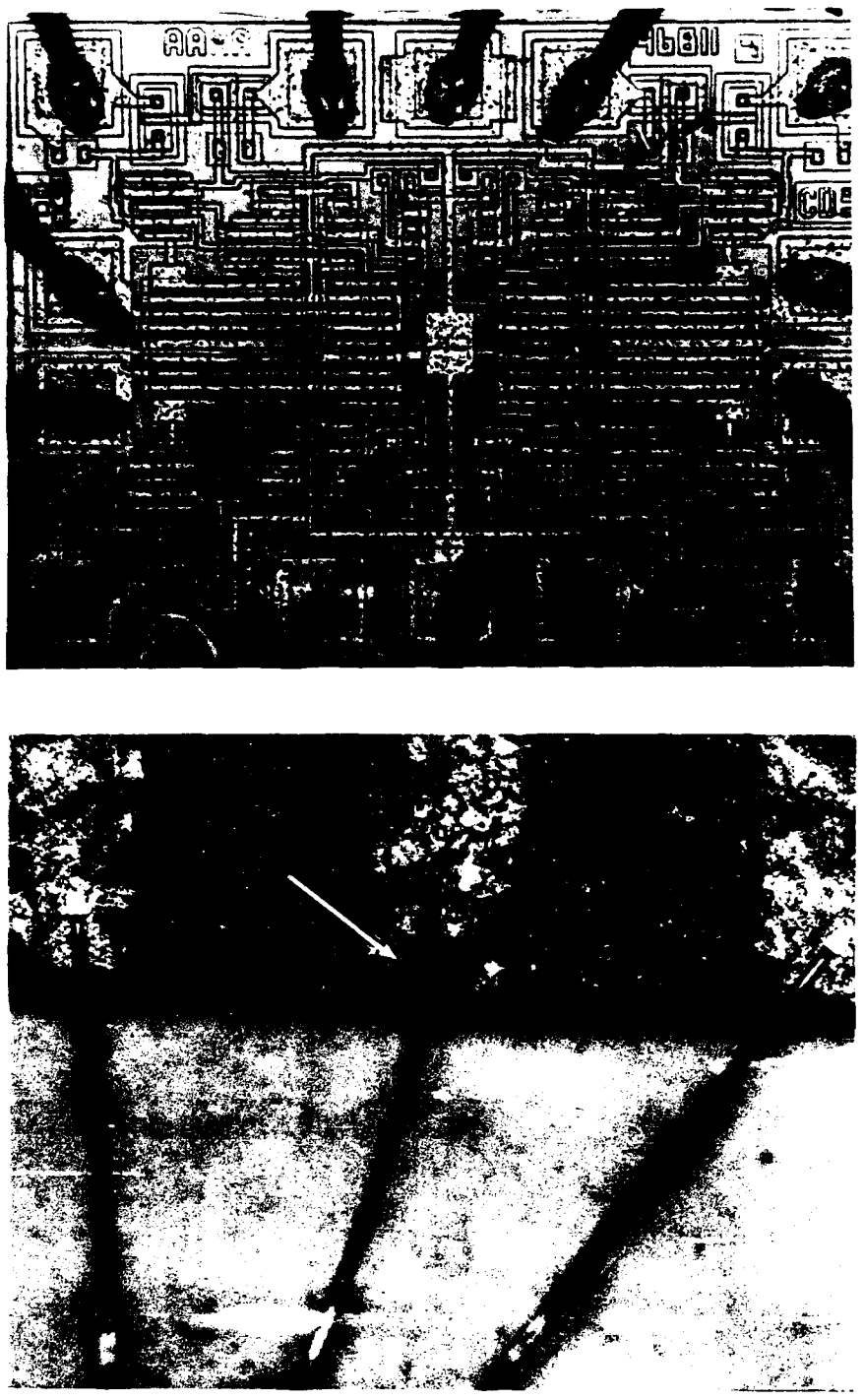


Figure 50. Die (top) and leadwire (bottom) appearance of coated D-package after 500 hours sequential autoclave exposure showing corrosion byproducts at the OLB on coated leadwire #14, s/n 103(50X).

HAST Exposure

Reliability test results from direct and sequential HAST exposures are shown in Figures 51 and 52. The HAST data clearly indicates that the reliability of coated D-packages far exceeds that of standard D-packages. A significant improvement in moisture and ion protection was obtained using the ceramic coatings.

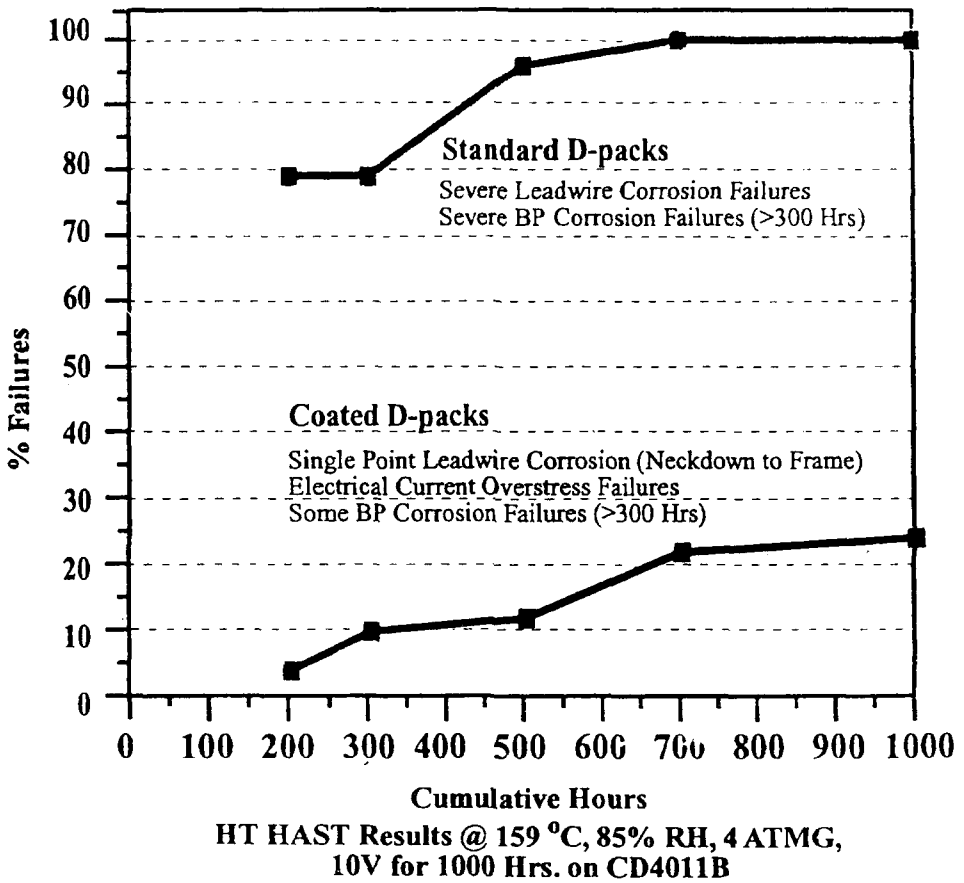


Figure 51. Graphic illustration of the reliability data on CD4011B CMOS devices in HAST.

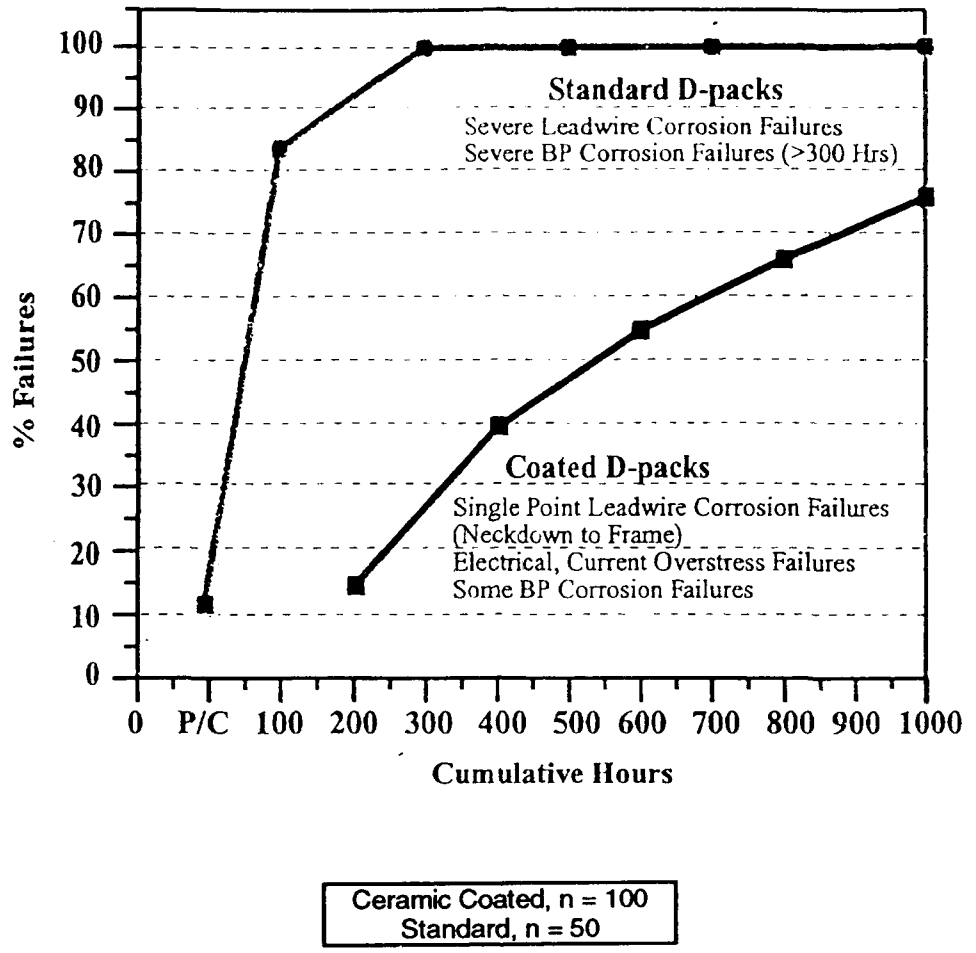


Figure 52. Graphic illustration of the reliability data on CD4011B CMOS devices in sequential HAST.

Direct HAST Exposure

Failure analysis of standard D-packages subjected to direct HAST exposure revealed severe corrosion at both V^+ and V^- bond pads, as shown in Figure 53. The failure mechanisms of coated D-packages were predominantly corrosion/aluminum dissolution of the V^+ bond pad but only at the region where the bond pad narrows down to a surface metallization trace (necking region), as shown in Figure 54. Electrical overstress and electromigration of aluminum have been suggested as a possible failure mechanism due to the presence of aluminum in the crystal structure of the silicon [25]. Leadwire corrosion at the OLB was also observed on a few devices. No change in failure mode was observed on the devices which failed after extended test periods (to 1000 hrs).

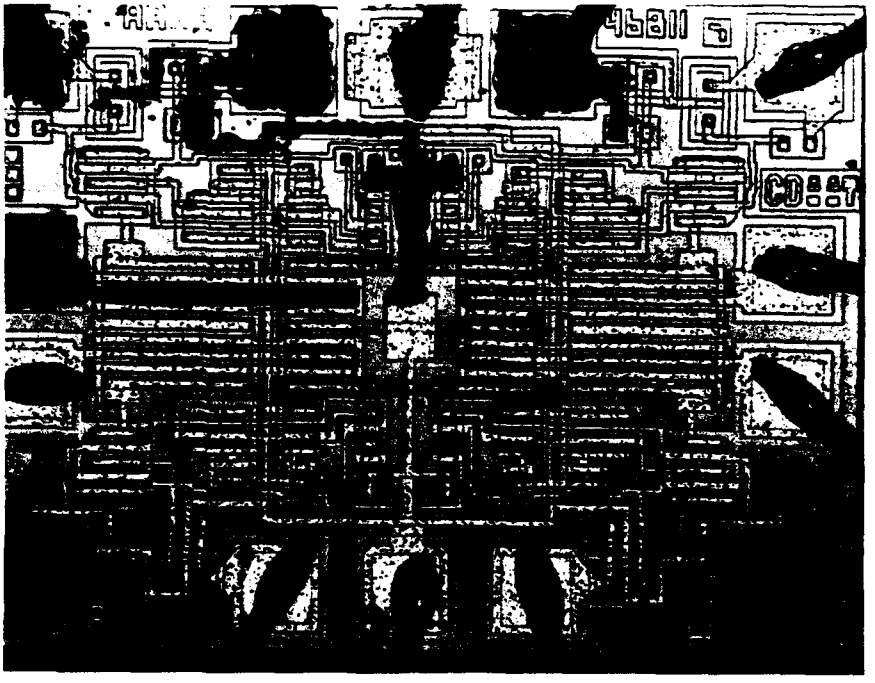
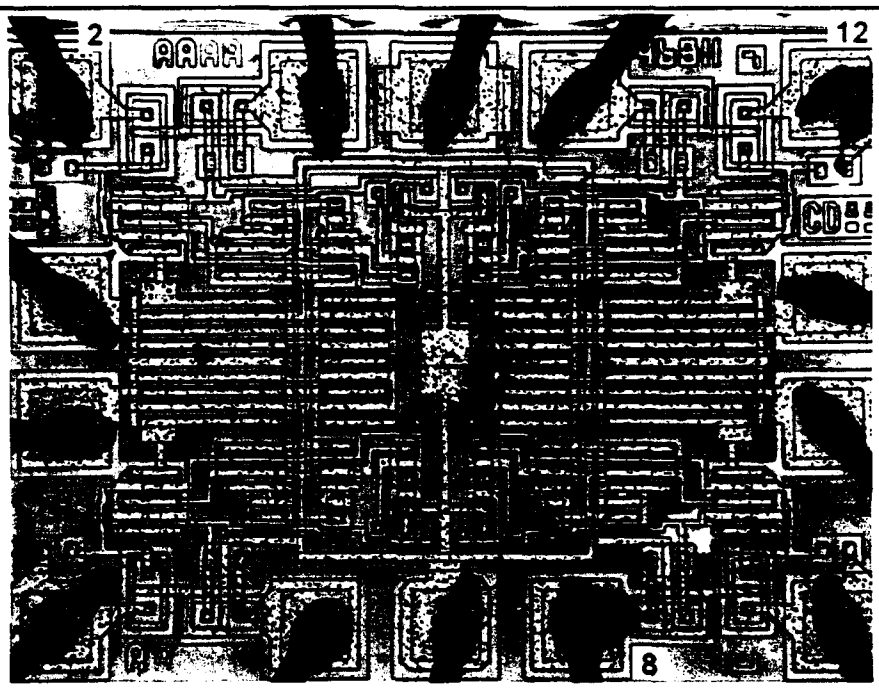
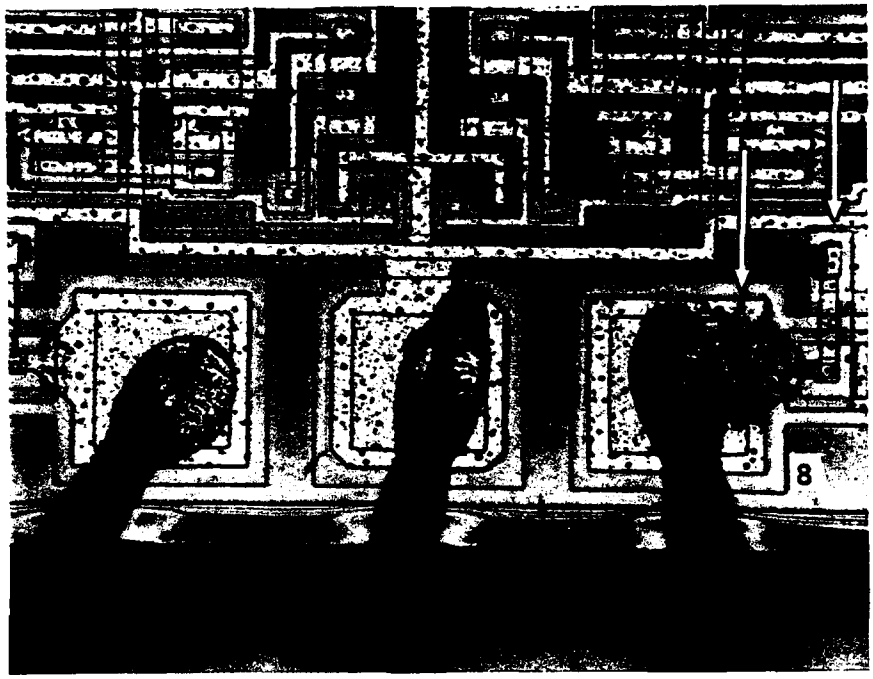


Figure 53. Whole die surface showing severe corrosion around V^+ and V^- pins; corrosion also observed on ground and output surface trace (pin 3); standard D-package after 200 hrs HAST exposure, s/n 028 (100X).



(a) Whole die surface showing corrosion at the necking region of the bond pad to surface trace at pins 2, 8, & 12 (100X).



(b) Close-up view of the die showing evidence of metal migration from the bond pad necking region to an internal protection diode (200X).

Figure 54. Coated D-package, s/n 100, after 300 hours of HAST exposure.

Sequential HAST Exposure

The comparative data illustrated between Figures 51 and 52 suggest that the preconditioning exposure accelerated the hazard rate of early failures in HAST for both standard and ceramic-coated D-packages in HAST.

Analysis of devices subjected to sequential HAST confirms that standard D-packages failed due to multiple open circuits caused by severe leadwire corrosion (swollen wires) on all aluminum wires as previously described in the preconditioning exposure alone. Failure analysis of coated D-packages revealed that early failures (100 hrs) were due to isolated single point leadwire corrosion at the OLB resulting from the fracture of coated leadwires unprotected from mechanical shock and vibration, as shown in Figure 55. As the test exposure progressed, the failure modes transitioned from isolated leadwire corrosion to aluminum migration from the bond pad necking region to the input protection diode, as shown in Figure 56. This is the same failure mode observed on the coated D-packages subjected to direct HAST exposure. Starting at about 800 hours, some coated D-packages failed due to conventional bond pad corrosion, as shown in Figure 57.

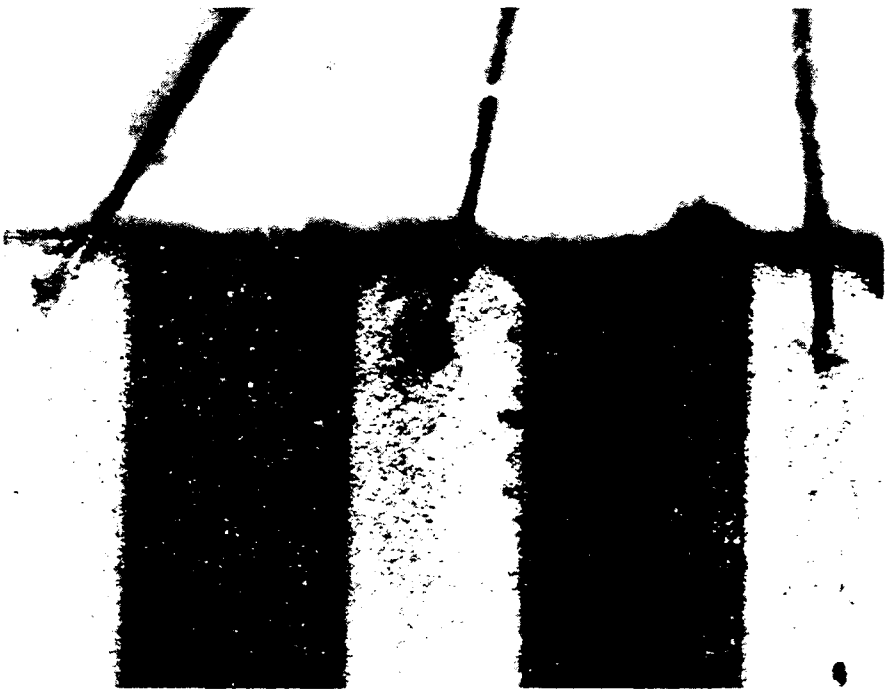
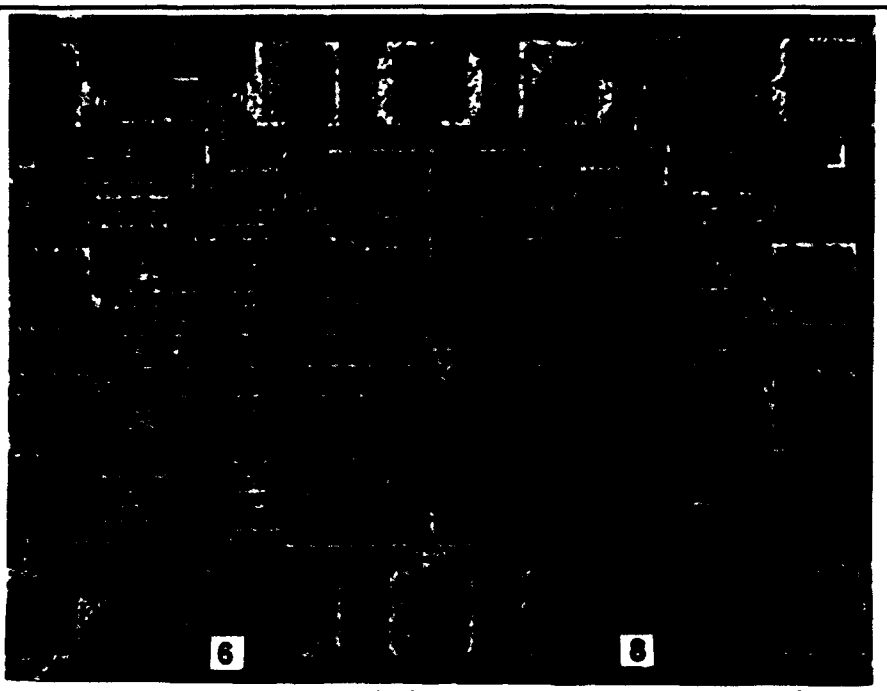
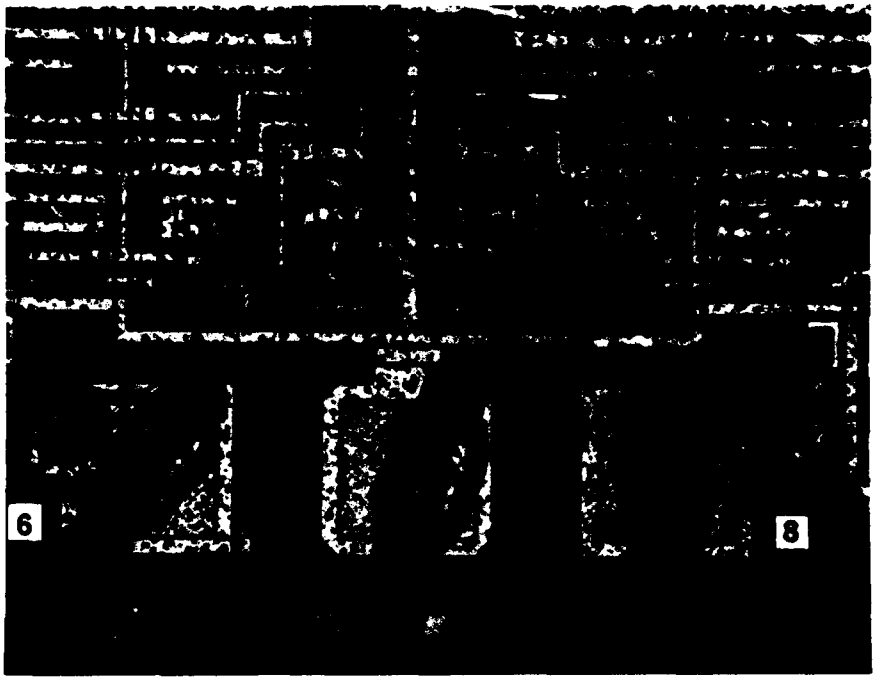


Figure 55. Corrosion byproducts of the aluminum leadwires at the OLB of pin 14; coated D-pack, s/n 246, after 100 hrs of sequential HAST exposure (50X).



(a) Whole die surface showing degradation at the necking region of the bond pad to surface trace at pins 6 and 8; (100X).



(b) Close up view of the die showing evidence of metal migration from the bond pad necking region at 6 and 8 to a protection diode; (200X).

Figure 56. Die of coated D-Pack, s/n 276, after 200 hours of sequential HAST exposure.

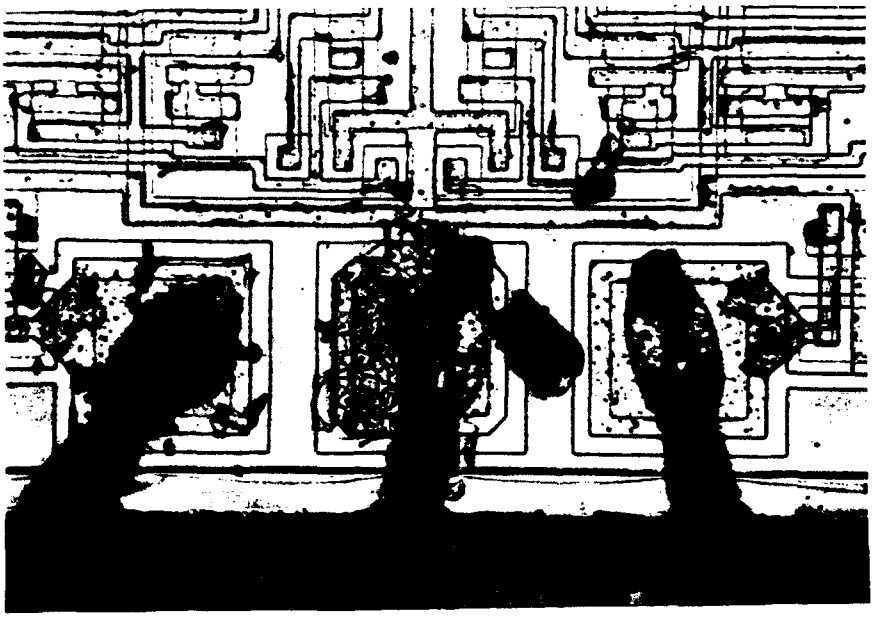


Figure 57. Close up view of bond pads 6, 7, and 8 showing both metal migration and corrosion of coated D-pack, s/n 238, after 1000 hours of sequential HAST exposure (200X).

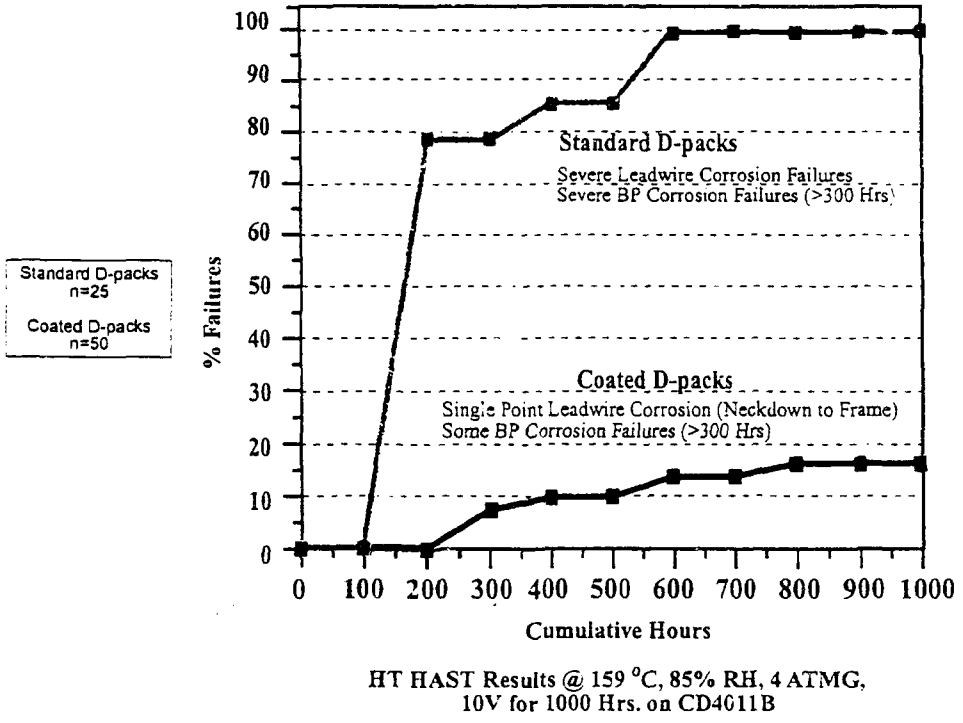
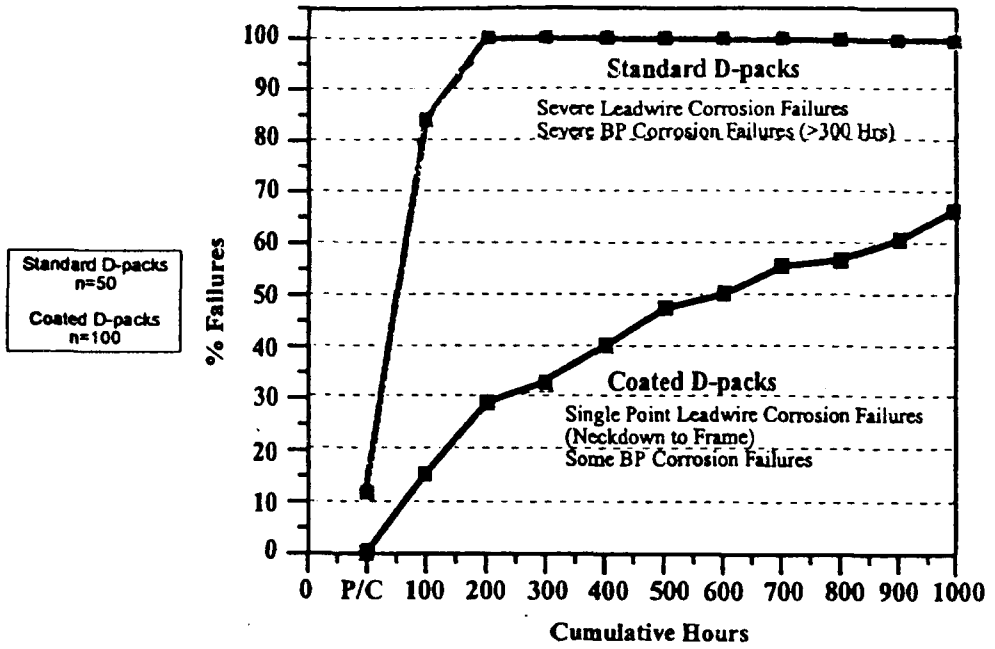


Figure 58. Corrected direct HAST data showing corrosion failures for CD4011B in open D-packages.



Sequential HAST Tests = 24 Hrs. Autoclave @ 121 °C, 100% RH: 200 Temp Cycles @ -65 °C to +150 °C: then HT HAST @ 159 °C, 85% RH, 4 ATMG, 10V for 1000 Hrs. on CD4011B

Figure 59. Corrected sequential HAST data showing corrosion failures for CD4011B in open D-packages

Sequential Temperature Cycling with Salt Fog

After 1000 cycles (hours) of temperature cycling, no additional signs of aluminum degradation were observed beyond that which was reported earlier from the preconditioning exposure. The devices were then subsequently subjected to salt fog exposure.

The reliability results from the sequential temperature cycling with salt fog are shown in Figure 60. The salt fog results indicate that the ceramic coatings protect the devices from corrosive ions (NaCl) if the coatings are continuous and free of pinholes or induced fractures.

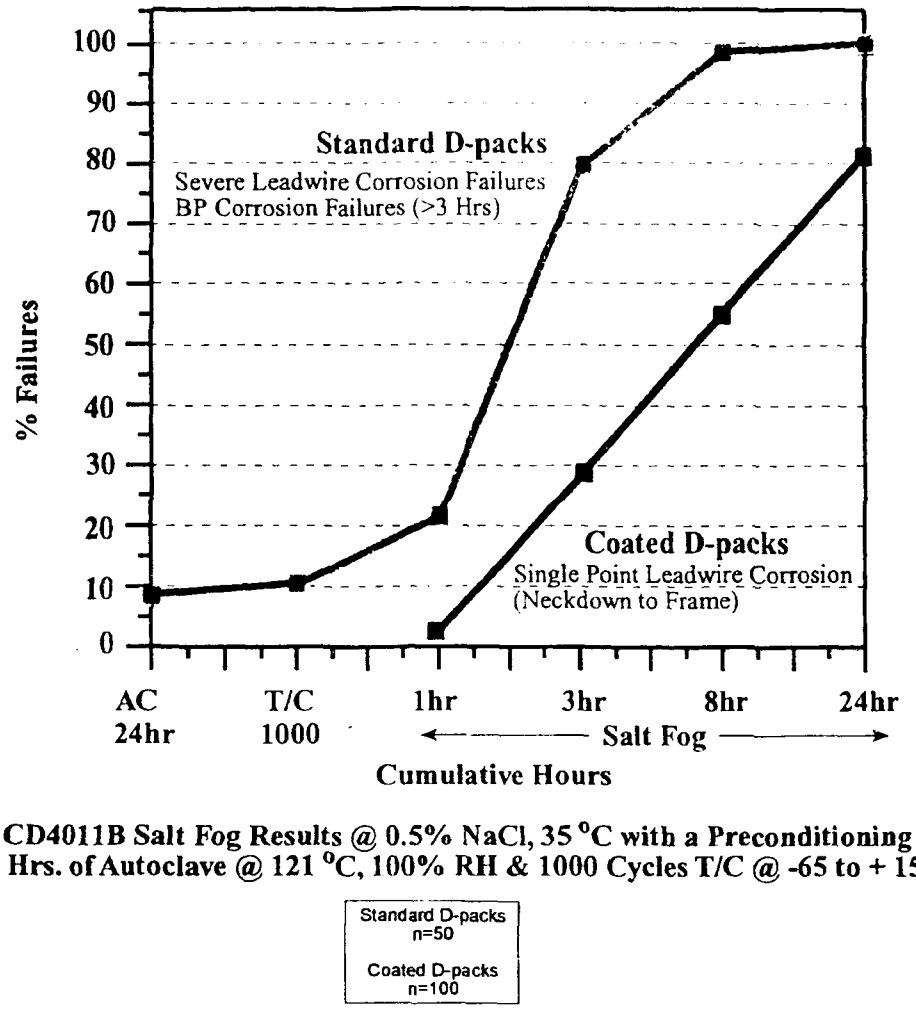


Figure 60. Graphic illustration of the performance data on CD4011B CMOS devices in sequential temperature cycling with salt fog.

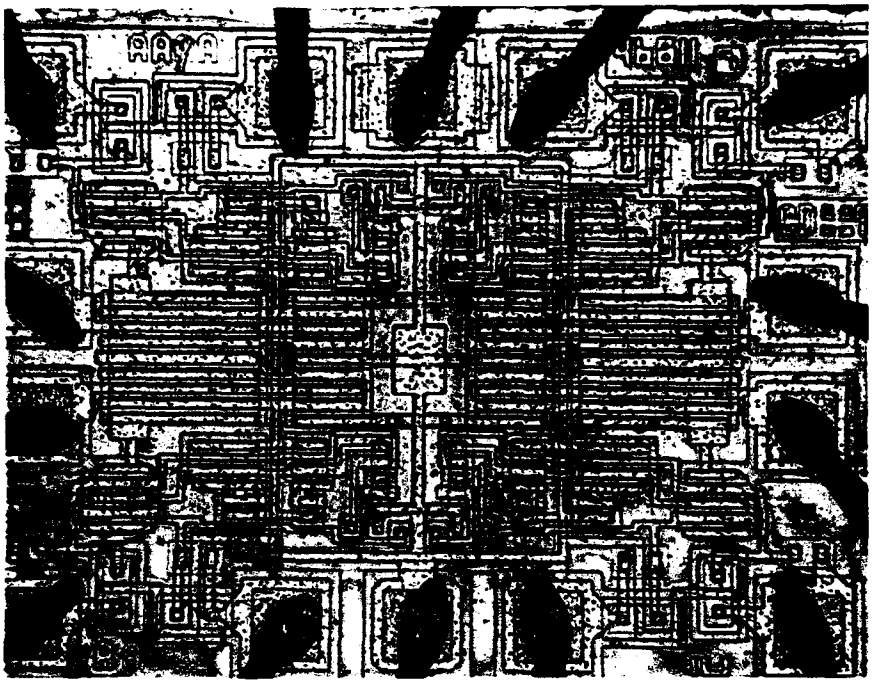
Analysis of standard D-packages prior to temperature cycling revealed severe leadwire corrosion (swollen wires) on all aluminum wires as described previously in the preconditioning exposure. No changes in device appearance were observed during the subsequent temperature cycling exposure.

Analysis of standard D-packages after salt fog exposure revealed severe leadwire corrosion which caused multiple open circuit failures. Analysis of coated D-packages revealed that the primary failure mode was isolated, single point leadwire corrosion at the OLB, as shown in Figure 61. The chip continues to look as good as when the device went into test, as shown in Figure 62.

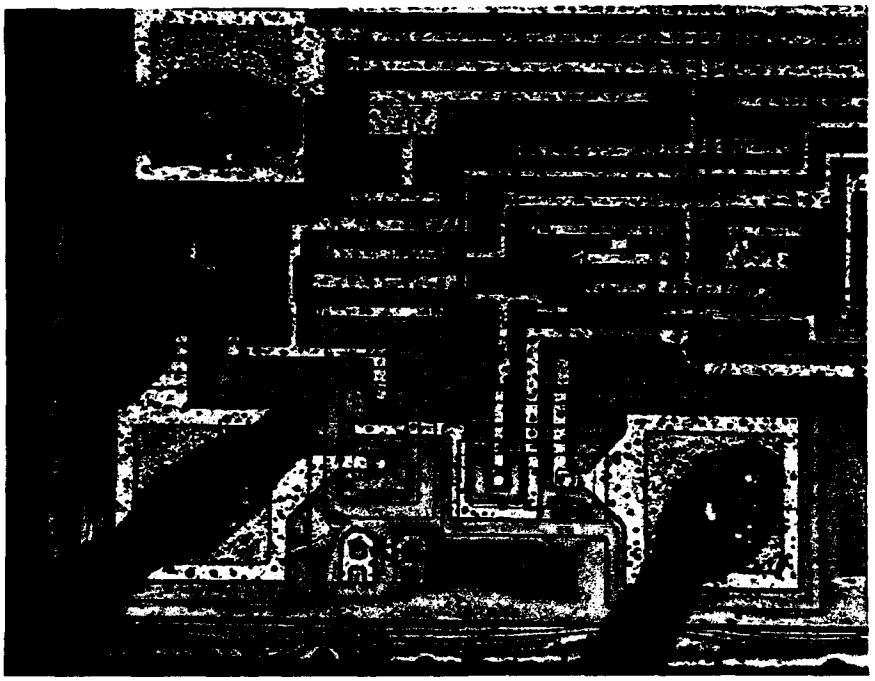
(a) Result of leadwire corrosion at the OLB (100X).

(b). Result of leadwire corrosion in the span of the wire (50X).

Figure 61. Leadwires of a coated D-Package, s/n 400, after 24 hours of sequential salt fog exposure.



(a) Whole die surface showing corrosion-free bond pads (100X).

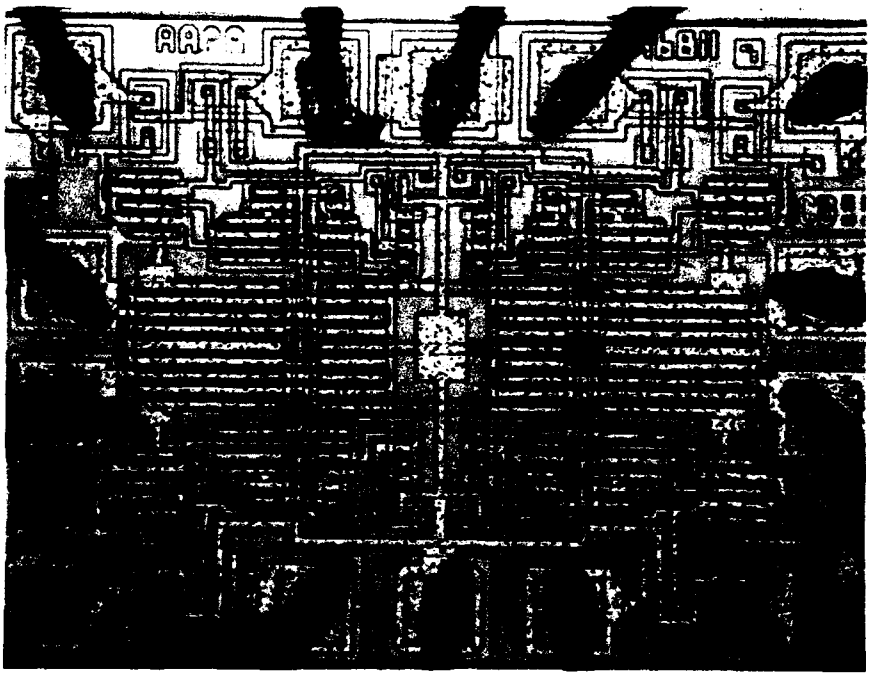


(b) Close up view of corrosion-free bond pads at pins 4, 5, and 6 (200X).

Figure 62. Die of coated D-Package, s/n 400, after 24 hours of sequential salt fog exposure.

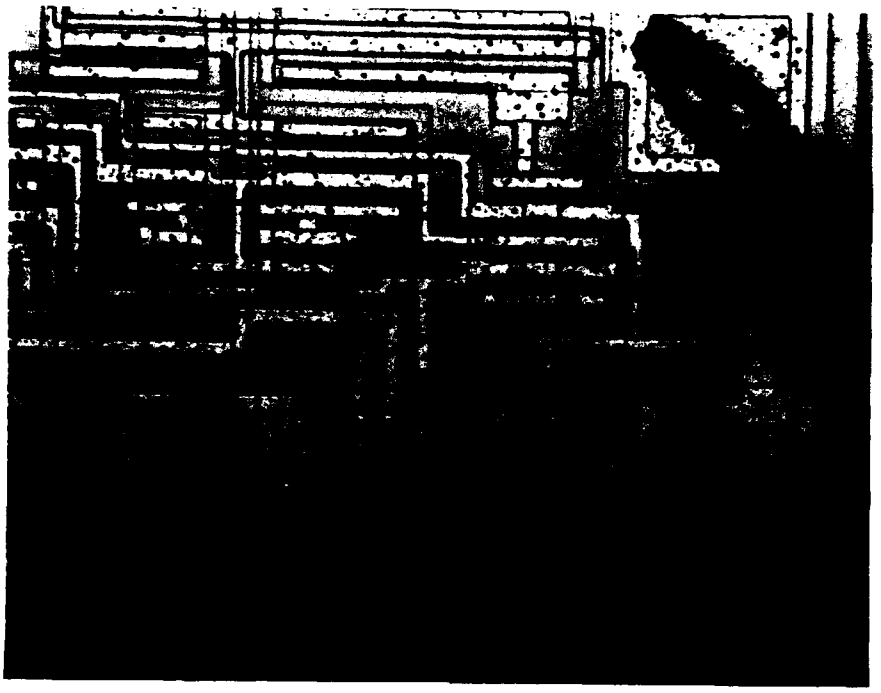
Analysis of Functional CMOS Devices After Reliability Testing

Randomly selected CMOS devices, which passed full electrical testing after completing the total reliability test program, were analyzed. With regard to comparing standard and ceramic-coated D-packages, only the ceramic-coated D-package devices survived the environmental stress testing to 1000 hours of exposure. A representative sampling of functional, coated D-package devices from sequential autoclave, HAST, and salt fog is shown in Figures 63 thru 65 respectively.

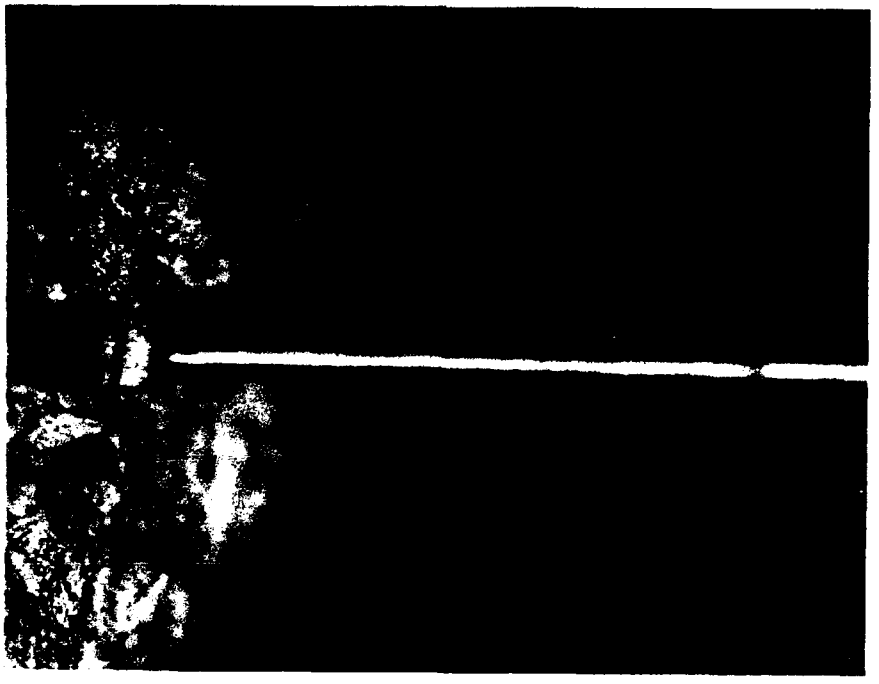


a) Whole die surface showing corrosion-free bond pads.

Figure 63. Appearance of die and leadwires of coated D-Package, s/n 199, after 1000 hours of sequential autoclave exposure

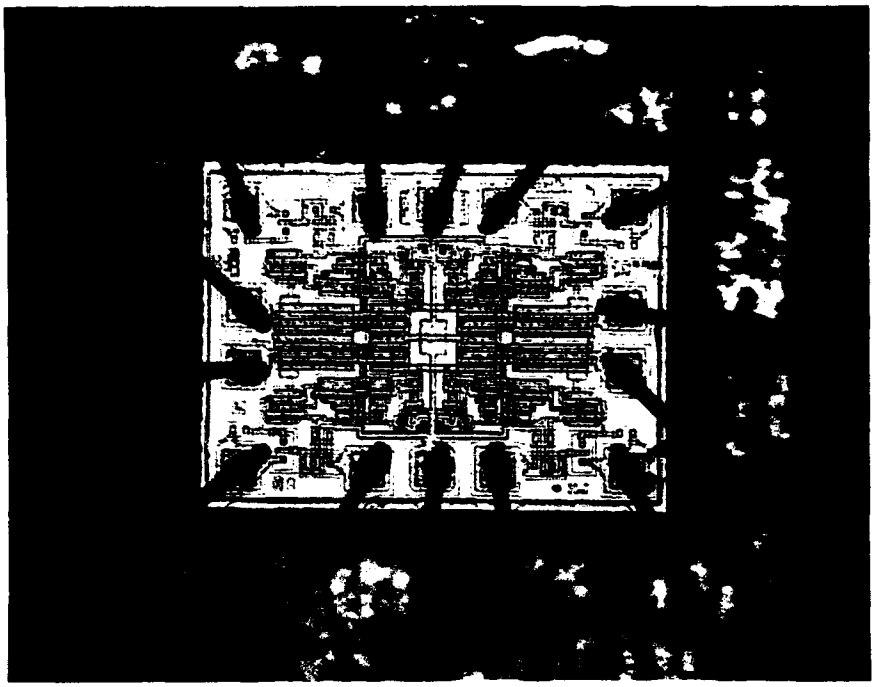


(b) Close up view of corrosion-free bond pads at pins 4, 5, and 6 (200X)

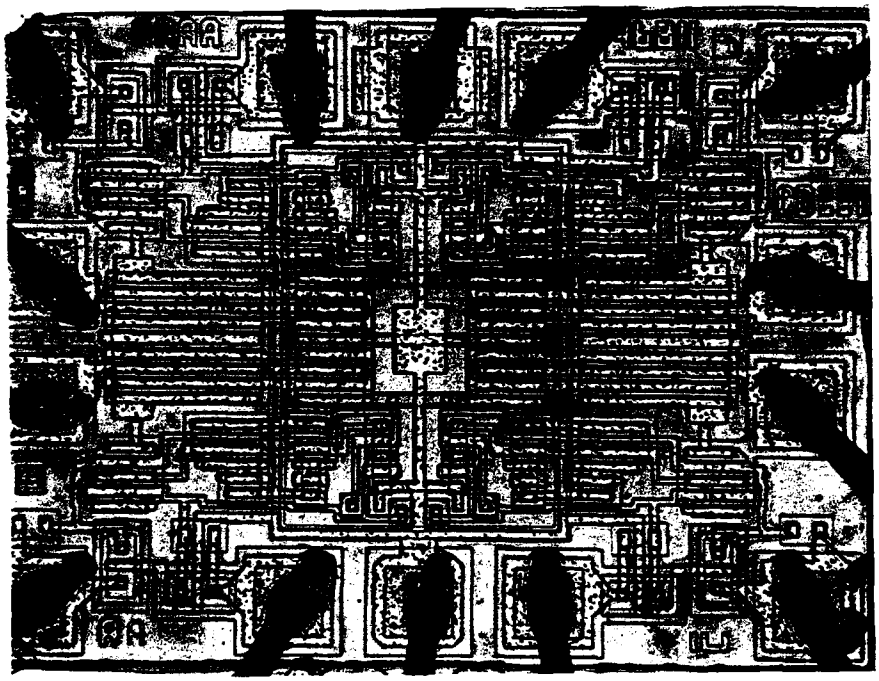


(c) Appearance of coated leadwire after 1000 hours of sequential autoclave (100X).

Figure 63 (cont.). Appearance of die and leadwires of coated D-Package, s/n 199, after 1000 hours of sequential autoclave exposure.

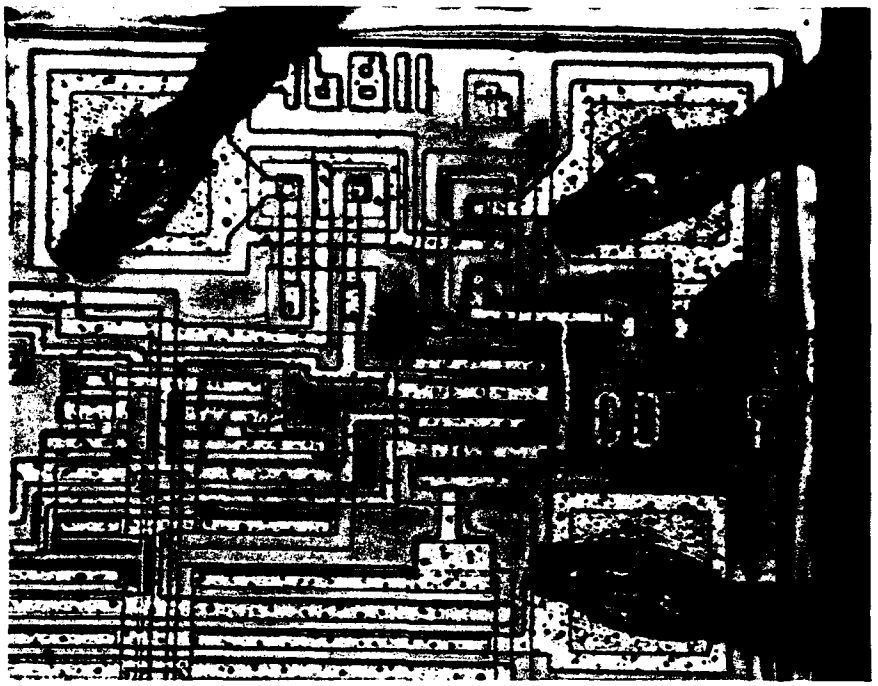


(a) Entire die assembly showing corrosion-free bond pads and leadwires (50X).

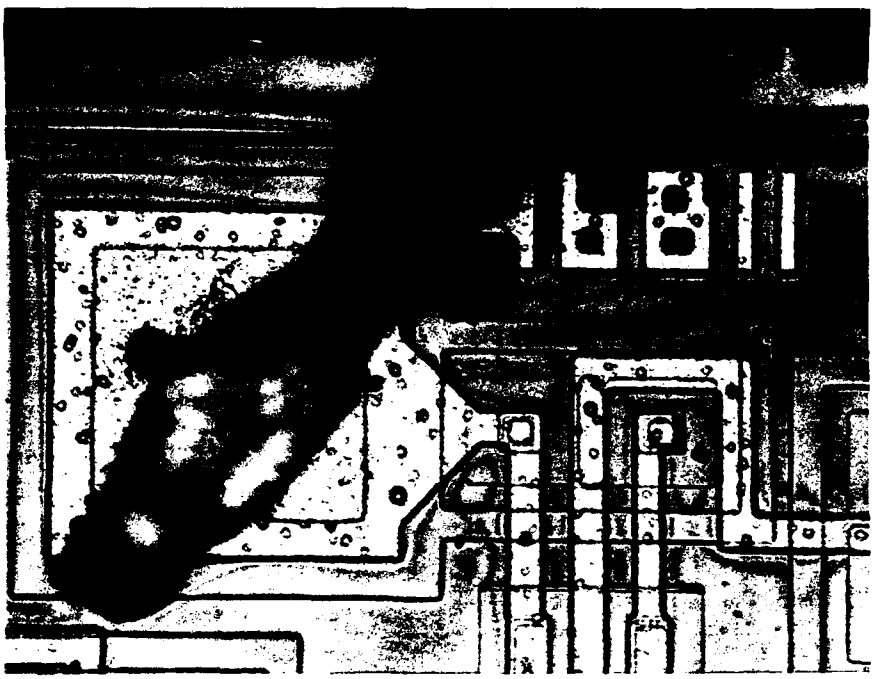


(b) Whole die surface showing corrosion-free bond pads and surface metallization traces (100X).

Figure 64. Appearance of die and leadwires of coated D-Package, s/n 257, after 1000 hours of sequential HAST exposure.

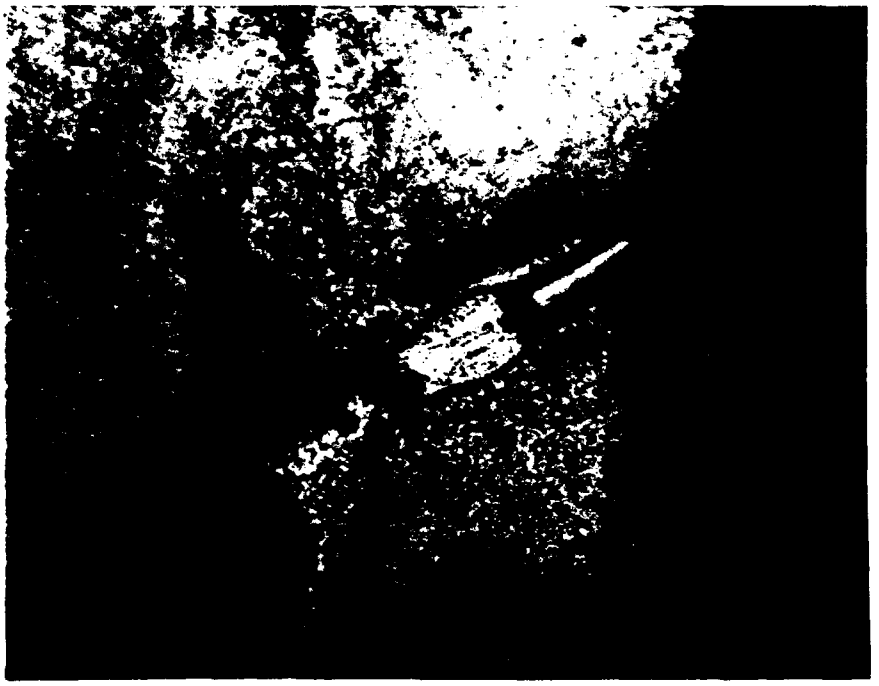


(c) Close up view of corrosion-free bond pads at pins 11, 12, and 13. (200X)



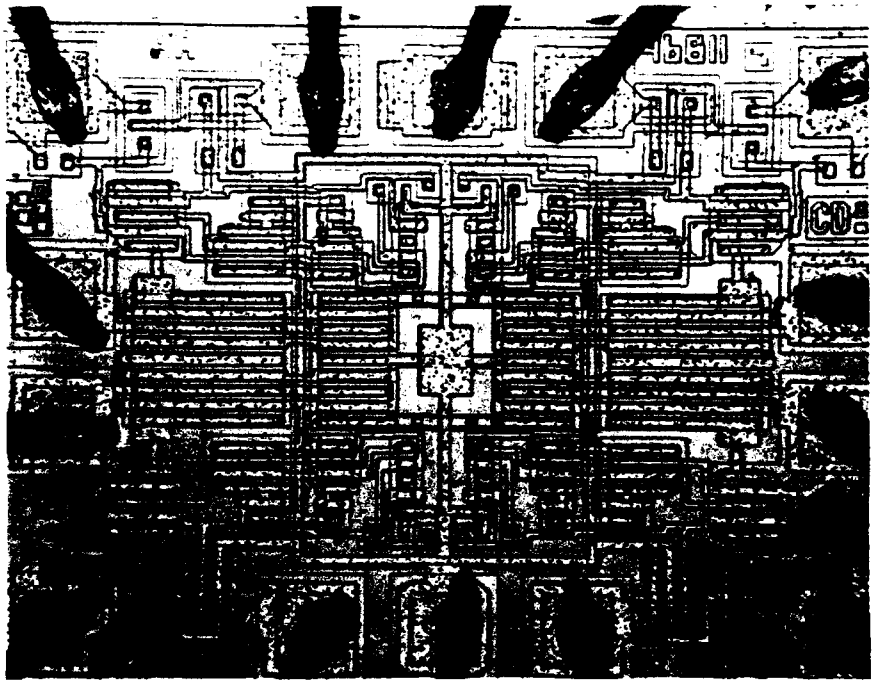
(d) High magnification view of corrosion-free bond pads at pin 13. (400X).

Figure 64 (cont.). Appearance of die and leadwires of coated D-Package, s/n 257, after 1000 hours of sequential HAST exposure.

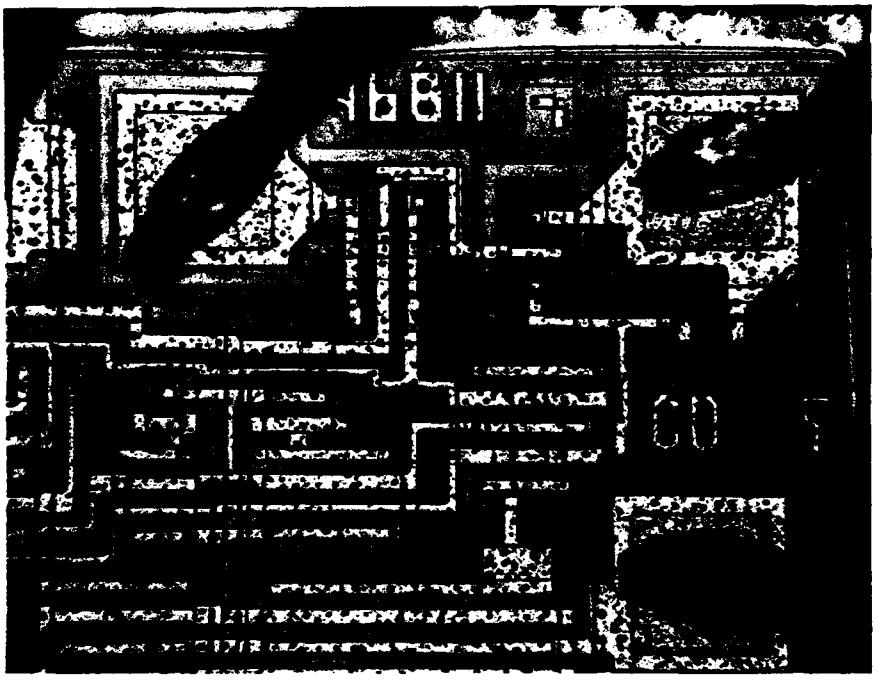


(e) Appearance of corrosion-free coated leadwire(200X).

Figure 64 (cont.). Appearance of die and leadwires of coated D-Package, s/n 257, after 1000 hours of sequential HAST exposure.

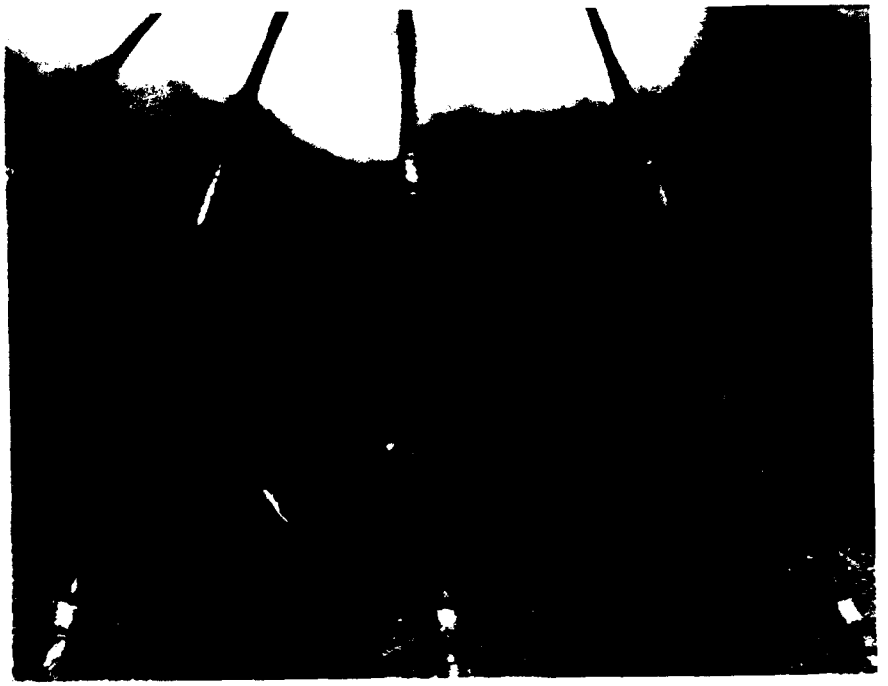


(a) Whole die surface showing corrosion-free bond pads. (100X).



(b) Close up view of corrosion-free bond pads at pins 11,12, and 13. (200X).

Figure 65. Appearance of die and leadwires of coated D-Package, s/n 312, after 24 hours of sequential salt fog exposure.



(c) Appearance of coated leadwire. (50X).

Figure 65 (cont.). Appearance of die and leadwires of coated D-Package, s/n 312, after 24 hours of sequential salt fog exposure.

Summary of CD4011B CMOS Device Reliability

1. The reliability in HAST of ceramic-coated die in plastic packages does not equal that of traditional hermetic packaging. However, it does approach the reliability of hermetic packages by over 600 hours in direct HAST exposure over standard plastic packaged devices.

2. Sequential and direct HAST exposures indicate that the reliability of ceramic-coated die in plastic packages surpasses the reliability of standard commercial plastic packaged devices by 300 and 600 hours difference, respectively, in time-to-first-failure.

3. A total of 1000 hours autoclave and temperature cycle / salt fog exposures did not differentiate the package reliability for the long term protection of plastic packaged ICs. The reliability of ceramic-coated die in plastic packages is equal to the reliability of standard die in plastic and hermetic packages after autoclave and temperature cycling / salt fog exposures.

4. Ceramic-coated devices and hermetically-packaged control devices consistently survived 1000 hours of direct and sequential reliability testing.

5. The application of the inorganic coatings did not adversely affect the electrical performance of the integrated circuit even after 1000 hours of sequential reliability testing.

6 An analysis of randomly selected functional CMOS devices exposed to 1000 hours of sequential HAST revealed that both coated PDIPs and hermetic package controls exhibited minor bond pad corrosion at biased (V^+) inputs. No standard PDIPs survived 1000 hours of sequential HAST.

LM124 Op-Amp Test Device

The reliability test results generated on the standard commercial CD4011B CMOS PDIPs indicated that the HAST exposure was the most differentiating environmental test used so far in this study. Neither 1000 hours of autoclave nor 1000 temperature cycles followed by 24 hours of salt fog provided adequate package differentiation, regardless of whether the devices had undergone a preconditioning exposure. Prior experience in the long term reliability of plastic encapsulated devices by National Semiconductor suggests that the limited autoclave and temperature cycling exposures, performed by Dow Corning, did not produce failures previously encountered in long term military field assessments. HAST, on the other hand, did induce both ion and moisture related failure mechanisms on the CMOS devices and would be the appropriate test condition for the LM124 Op-Amp.

LM124 device failures are defined as a non-functional op-amp that is attributable to either moisture or ion-induced corrosion of any area of the die. Examples of conditions not considered failures include electrostatic discharge (ESD), electrical overstress (EOS), package related leakage current, board assembly (solder) degradation, etc.

A description of the test device configurations referred to throughout this portion of the reliability testing and failure analysis are as follows:

(Plastic & Hermetic)

Abbreviation	Description
Standard TapePak™	Standard die (no die coat) in plastic packages.
Ceramic-coated TapePak™	Ceramic-coated die in plastic packages.
Control	Standard die in hermetically sealed packages.

Abbreviation	Description
Standard PDIP	Standard die (no die coat) in plastic packages.
Ceramic-coated PDIP	Ceramic-coated die in plastic packages.
Control	Standard die in hermetically sealed packages.

LM124 Test Vehicles

To assess the performance of the TapePak™ and ceramic coating technologies, the following LM124 test vehicles were used:

• Standard 40-lead TapePak™ (uncoated)	100 units
• Ceramic-coated 40-lead TapePak™	100 units
• Hermetic 14-lead DIP control	100 units
• Standard 14-lead PDIP (uncoated)	24 units
• Ceramic-coated 14-lead PDIP	24 units

The LM124 PDIP test vehicles were funded by National Semiconductor to provide a correlation with other HAST performance data for the LM124.

LM124 Reliability Test Flow Strategy

The reliability test flow for the LM124 Op-Amps included a preconditioning sequence followed by HAST exposure at 140°C for 1100 hours. This test flow is different than that used for the reliability testing of the CMOS devices and is based on the following strategy.

Preconditioning Exposure

The purpose of this preconditioning is to simulate the manufacture, storage, and assembly processing of military-grade SMT devices. Preconditioning is used as a screen in industry for many commercial surface mounted devices because of the effects of the component board mounting process.

Standard plastic-encapsulated components will always absorb moisture, whether by capillary action along an interface or from diffusion through the molding compound. Much work has been performed by National Semiconductor regarding the moisture penetration and saturation of epoxy molding compounds and plastic components [26]. Under the right conditions, a plastic component may completely saturate in a relatively short time, i.e. days. Under saturation conditions, moisture tends to collect at the interfaces between the epoxy molding compound and either the die or die paddle [27,28]. This provides a dangerous situation for surface mountable components.

The nature of surface mount is the mounting of components on a printed circuit board via a hot bar reflow process, which applies large amounts of heat for a relatively short time to the leads to reflow the solder and mount the component. This exposes the component to high levels of heat energy which may vaporize any collected moisture and cause either delamination or a popcorning effect, where the molding compound physically separates from the interface and causes a package crack, thereby jeopardizing the package integrity. A number of steps can be taken to avoid this problem, including designing for better package ruggedness, baking to dry out the parts, and packing components in hermetic bags with dessicant for short term storage. Preconditioning is used as a screen for surface mounted components to determine if a component should be drypacked or not. The intent is to provide conditions that would induce package cracking or delamination [29].

HAST Exposure at 159°C vs. 140°C

HAST is a temperature, humidity, pressure, and bias environmental stress test that has been used in the past to evaluate the moisture reliability of electronic components. Currently, HAST is not widely used in industry, but has been the focus of a number of research programs to provide a better moisture reliability screen than traditional 85/85 testing (85°C,85%RH).

There has been much debate over the appropriate temperature to perform HAST. There are those who feel that any reliability test performed above 125°C, which is typically the maximum operating temperature for which a device is designed, does not reflect realistic field operation. Others feel that the temperature should be maximized to achieve the benefits of a higher acceleration factor to failure relative to a known failure mechanism. In determining the appropriate test temperature, many considerations must be made of the materials present, the application, the type of data desired, as well as any prior art for the component or HAST conditions specified.

HAST at 159°C was performed by Dow Corning on the CD4011B test vehicles. Although this test condition does not represent real field service conditions, this exposure will force any ionic impurities from the packaging materials (EMC) to the die surface. This presents a unique opportunity to thoroughly assess existing and new advance packaging materials and processes for long term device reliability. In the case of Dow Corning, the ion and moisture barrier properties of the ceramic coatings

are readily validated. Much of Dow Corning's previous HAST data was also obtained at 159°C, which, for correlation purposes, allowed its use as baseline information on the CD4011B devices [4,8,15].

National Semiconductor currently runs HAST at two different temperatures, 131°C and 135°C. Most of the IC manufacturers and users do not exceed 140°C HAST exposure in their qualification or screening programs. It has been found that 140°C HAST produces reliability data with service related failure mechanisms for meeting todays just-in-time manufacturing requirements. There are also equipment limitations on some of the HAST chambers due to their pressure rating. The reliability assessment of the LM124 Op-Amp was performed using HAST, as per JS-22, at 140°C to maximize the acceleration of time-to-failure without exceeding recommended equipment limitations and inducing extraneous failure modes.

Reliability Testing

All LM124 test vehicles were exposed to the preconditioning sequence. The 40-lead TapePak™ devices, both standard and ceramic-coated, were exposed and tested with their molded carrier ring. The preconditioning flow used for the LM124 test vehicles in this program consisted of the following steps. These steps were developed jointly by National Semiconductor, Dow Corning, and Rome Laboratory to simulate the military storage environment.

- Burn-in for 168 hours at 125°C.
- Room temperature electrical testing.
- Vapor Phase Reflow Oven exposure at 219°C for 40 seconds.
- Visual inspection and room temperature electrical testing.
- Temperature cycling, as per Mil-Std-883, Method 1010, -65°C to 150°C, Condition C, for 200 cycles.
- Visual inspection and room temperature electrical testing.

Visual Inspection Criteria

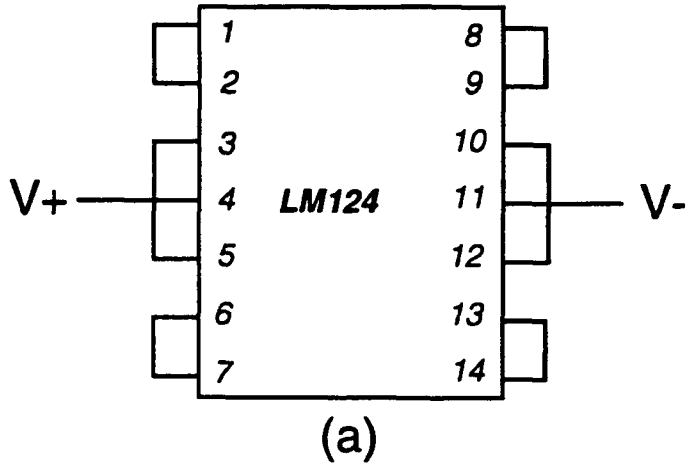
For the purposes of this program, the visual inspection criteria for the preconditioning included general physical appearance of the exterior of the package and cracks in the epoxy molding compound visible up to 20X.

HAST at 140°C

After preconditioning exposure, the LM124 test vehicles were subjected to 1100 hours of HAST exposure. HAST was performed as per JEDEC specification, JS-22, Method A110, Code C, at 140°C. The test vehicles were removed at specified periods during the test for visual inspection and electrical testing. These intervals were at 100, 362, 500, 700, 900 and 1100 hours. These parts were visually inspected for any damage or degradation to the external package or leads. The parts were cleaned and dried out to help eliminate false parametric shifting caused by moisture leakage between pins. This was a concern with the TapePak™ parts, as they are fine-pitch and are more susceptible to this condition. This procedure was instituted after 100 hours HAST exposure because of a large number of initial parametric failures. All parts were electrically tested using a production test program and tester.

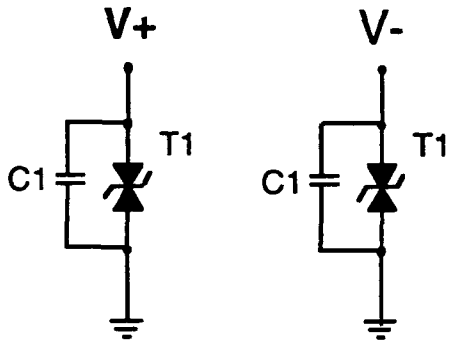
Biasing of LM124

Figure 66a shows the biasing diagram for the LM124. Pins 1,2,3 correspond to Amplifier #1; Pins 5, 6, 7 correspond to Amplifier #2; Pins 8, 9, 10 correspond to Amplifier #3; Pins 12, 13, 14 correspond to Amplifier #4. Each device was protected using the circuit protection schemes shown in Figure 66b.



(a)

Each device utilizes the following circuit protection schemes:



(b)

Figure 66. Schematic of HAST Biasing of the LM124 Test Vehicles.

Conversion Boards

For the HAST testing, all the TapePak™ components were excised from their carrier ring and mounted onto a surface mount conversion board, which allowed the part to be inserted into a 14-lead DIP socket. The boards were designed to have the same pinout as the LM124 14-lead DIP components. This allowed the devices to be tested using the same tester and HAST boards.

National Semiconductor currently tests all fine-pitch surface mount devices using conversion boards to eliminate lead damage concerns and allow multiple testing insertions. At 2.3 mils thickness, the fine-pitch packages are very susceptible to lead damage via test handling. This arises from the lack of proper socketing for most small outline packages. Recent advances in z-axis conductive adhesives may allow parts to be tested with minimal lead damage. For this program, it was deemed that the best way to overcome the issue was to continue mounting the parts onto conversion boards.

Figure 67 shows a 40-lead TapePak™ device mounted onto a conversion board. These boards are used for the following advantages:

- Reduce damage to surface mount leads and allow multiple insertions.
- Mimic device field use, i.e. on printed circuit boards using SMT.
- Allow the use of existing 14-lead DIP test sockets and HAST boards.

The boards were constructed from laminated polyimide printed circuit board material with copper traces. The traces were then plated with solder for better wetting of solder during the component mounting operation and solder dip operation. Copper pins were soldered to the perimeter of the board to provide the electrical contact with the test socket. These pins were coated in a solder dip operation with eutectic Sn-Pb solder.

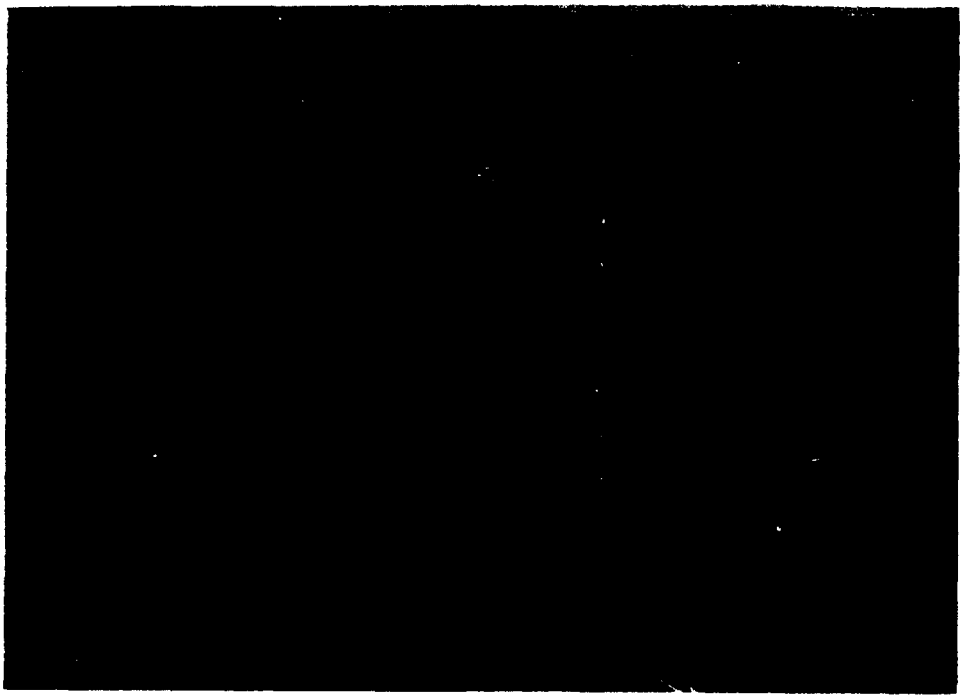


Figure 67. 40-lead TapePak™ Device Mounted on Polyimide Conversion Board to Emulate 14-lead DIP Pinout.

Plastic and Hermetic Packaged LM124 Devices

Failure analysis was performed on a representative sampling of the failed LM124 TapePak™. This was done by electrically rescreening all suspect failures using a benchtop curve tracer and a linear device hand tester designed specifically for the LM124. This tester allowed the investigation of each individual Op-Amp or the device.

Visual inspection of the devices throughout HAST testing showed visible degradation of the conversion boards for the TapePak™ devices. Figure 68 shows the change in appearance of the conversion boards as the testing progressed. This was evident on all TapePak™ devices, both standard and ceramic-coated, which were mounted on the conversion boards. The conversion board also exhibited a selective degradation that seemed to follow the biasing scheme of the device. Biased (V^+) conversion board traces were discolored (blackened); eventually, the entire board became discolored after extended exposures. There seemed to be no correlation between this phenomenon and detected device failures for the TapePak™.

The program defined a failure as a non-functional Op-Amp that is attributable to either moisture or ion-induced corrosion of any area of the die. The hand tester was used to screen all of the suspect failures for non-functioning Op-Amps. Any suspect failure that did not show a non-functioning Op-Amp, was not considered a test failure. These devices were not returned to test due to the potential for chamber contamination.

Devices that showed at least one non-functioning Op-Amp were investigated further to find its cause. Devices were grouped by the failed amplifier quadrant. A representative sample of each group was selected for investigation. These parts were analyzed closely to help determine if the failure was attributable to the die or the package. Parts were decapsulated using hot sulfuric jet etch or mechanical methods after analysis to show any signs of corrosion. Damage due to either mechanical or chemical decapsulation was not considered a failure.

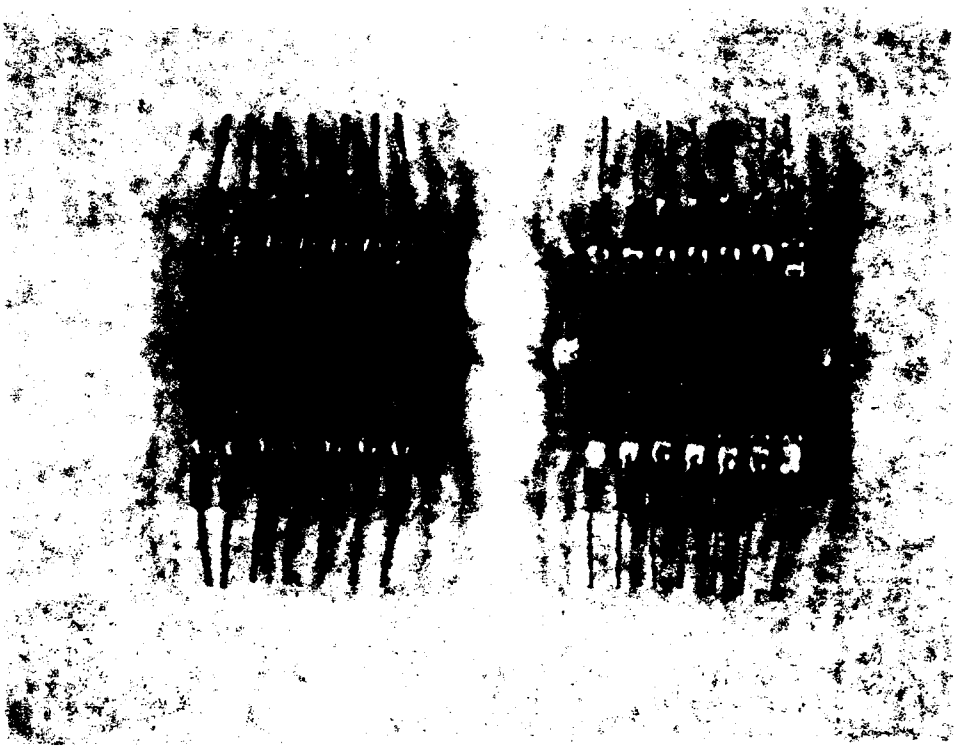


Figure 68. Difference in Appearance of TapePak™ Conversion Boards at 100 and 1100 Hours HAST Exposure. 1X.

LM124 Failure Analysis Findings

After analysis of the LM124 suspect failures, only one part was found to have exhibited a corrosion or moisture related failure. Aside from that part, no additional device failures were detected through 1100 hours of HAST at 140°C.

All of the suspect failures found through electrical testing were attributable to one of the following:

- parametric shift due to leakage currents induced by residual moisture within the package during test,
- parametric shift due to leakage currents across traces or leads on the TapePak™ conversion boards,
- parametric shift due to contact resistance between package leads and test socket,
- opens due to voiding or failure of conversion board solder joints,
- catastrophic failure due to corrosion in the field area of the die.

Of the aforementioned list, only the last bullet satisfies the definition of failure for this program.

Electrical testing of the LM124 after 362 hours exposure showed a failure of Amp #4 to function on s/n 264B, a standard LM124 TapePak™. Further investigation into the cause of failure showed no problems related to the conversion board. After decapsulation, an area on the die was shown to exhibit signs of corrosion. Figure 69 shows a 400X magnification photomicrograph of the area in question. It is evident from this photo that some of the die metallization is darker in some areas than others and seems to have spread from a single source. This may be evidence of moisture related corrosion of aluminum. Further investigation by SEM shows that the corrosion arose from a hairline crack in the primary passivation -- one that would not be detectable during a standard visual inspection of the die. The flaw appears to have been random and a result of the sharp corner that can pose problems to the deposited oxide and nitride films.

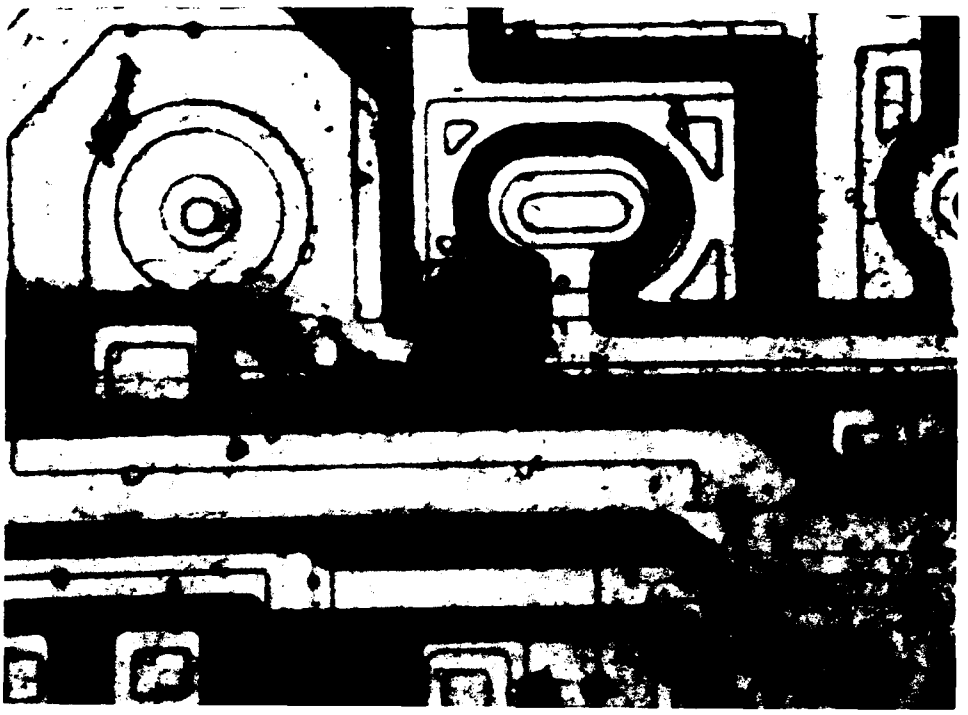


Figure 69. Field Area of Die on Standard 40-lead TapePak™ Device after 362 Hours HAST Exposure Showing Corrosion of Trace, s/n 264B. (400X).

A number of failures were attributable to breakdown of solder joints on the conversion board. Many failures were corrected on the tester by applying pressure at the solder joint to reestablish an electrical connection. Figure 70 shows pin 9 on s/n 141A, a ceramic-coated TapePak™ device which failed at 700 hours. The initial electrical test showed a continuity failure at pin 9. Further investigation showed an intermittent failure, which is often attributable to corrosion. However, when the leads were inspected closely, a large void was found in the solder joint, as shown in the photograph. Pressure applied to the lead reestablished the electrical contact. Therefore, these devices were not considered failures, as the device was still functional.

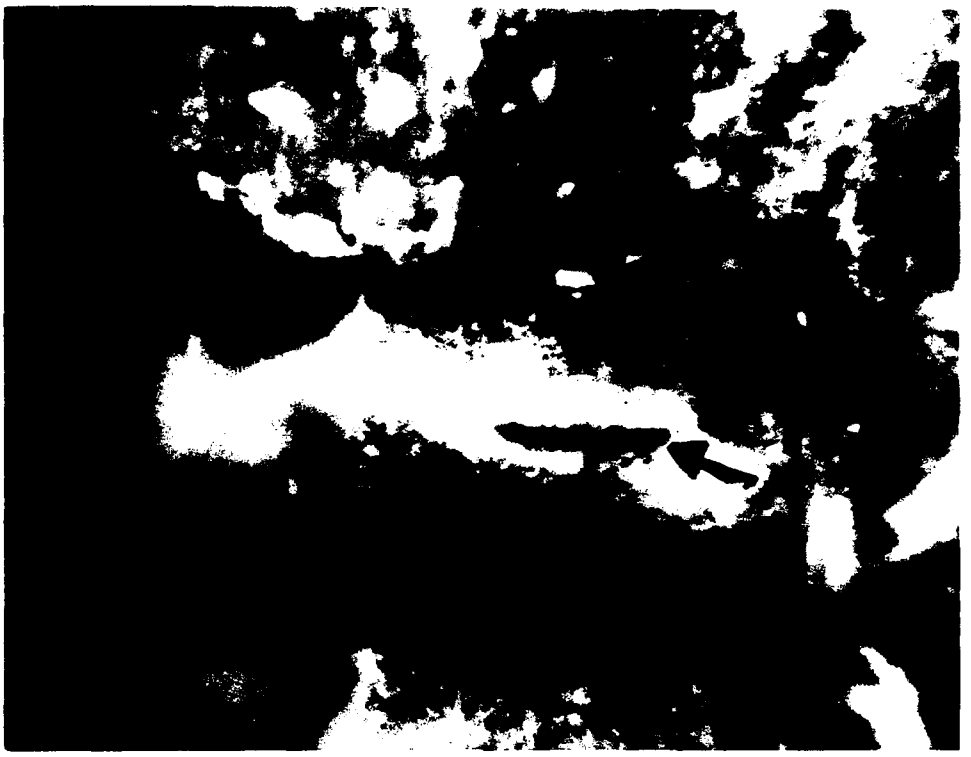


Figure 70. Conversion Board Solder Joint, Pin 9, Showing a Void Responsible for Electrical Test Failure. (35X).

Leakage between traces on the TapePak™ conversion boards for HAST was evident upon inspection of the boards. In many cases, the copper traces showed evidence of copper migration between the Op-Amp input and either V^+ or V^-. Figure 71 shows an example of copper migration. These leakages can account for non-functioning Op-Amps that would otherwise be functional.

Figure 71. Conversion Board Trace at Op-Amp Input and V+ Showing Copper Migration. (28X).

As the HAST testing progressed, visual inspection showed the condition of the conversion board leads deteriorating. A high number of failures were detected at 900 hours HAST exposure for both standard and ceramic-coated TapePak™ devices. This proved to be puzzling since almost all failures were parametric in nature, and therefore not a moisture-related die failure. Further investigation by examining a few of the suspect failures showed that there was a contact resistance problem related to the degradation of the conversion board. Surface oxidation of the leads by 900 hours was quite bad. Given the number of insertions these parts saw at this point, it is almost expected that some contact problems can arise. The production test contacter is designed to test parts with minimal damage to freshly soldered leads, which can pose problems when there is even the slightest amount of lead corrosion. This would account for the inordinate amount of failures at 900 hours. This does not fall within the realm of this experiment because the suspect failures are not attributable to any moisture or ion-related corrosion of the die.

There seemed to be no visible trends to indicate a significant difference in electrical or reliability performance between standard commercial and ceramic-coated LM124 devices. It is interesting to note that the LM124 TapePak™ devices, both standard and ceramic-coated, exhibited more fallout due to parametrics than the LM124 PDIP devices. Although these were parametric in nature, it does seem to indicate a difference in performance. This may be attributable to the use of PCB conversion boards, as these were only used on the TapePak™ devices. The PCB conversion boards represent the best available technology for testing of fine-pitch surface mount TapePak™ devices. However, the stringent demands of the long term reliability testing used in this experiment surpassed the capabilities of the boards. This may preclude their use in such long term testing in the future. Some of the analysis performed indicated that many of the failures were due to either solder joint degradation or leakage current across traces on the conversion board.

Table 11 shows the HAST reliability results. These numbers represent failures, as defined previously, after performing failure analysis of suspect failures.

Table 11. Reliability Data of LM124 Devices in HAST

Hours =>	100	362	500	700	900	1100
Hermetic Controls	0/100	0/100	0/100	0/100	0/100	0/97
Standard TapePak™	0/98	1/98	1/93	1/89	1/86	1/14*
Ceramic-coated TapePak™	0/99	0/87	0/83	0/79	0/78	0/13*
Standard PDIP	0/24	0/24	0/24	0/24	0/24	0/23
Ceramic-coated PDIP	0/24	0/24	0/24	0/24	0/24	0/24

** High fallout of parametrics attributed to HAST board solder breakdown.*

Given the results of the failure analysis, it was found that no failures were detected through 1100 hours of HAST exposure for the standard PDIPs, ceramic-coated TapePak™ and PDIPs, and the hermetic controls. There was only one failure found, at 362 hours, for the standard TapePak™ devices through 1100 hours of HAST exposure. Figure 72 shows the comparitive cumulative failure in percent for the standard and ceramic-coated PDIPs, and the hermetic control DIPs. Figure 73 shows the comparitive cumulative failure in percent for the standard and ceramic-coated TapePak™ devices and the hermetic control DIPs.

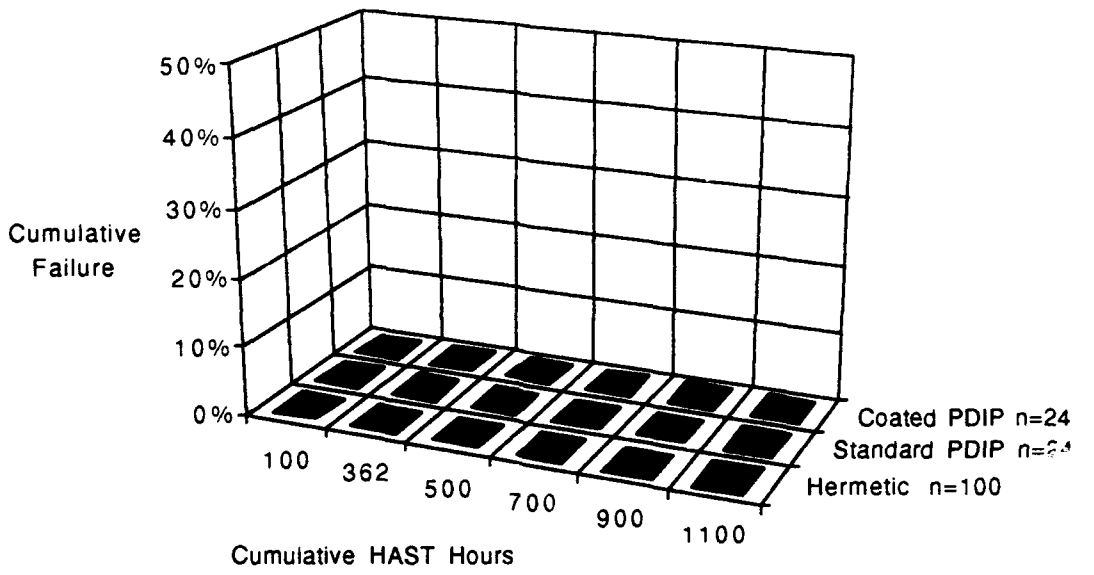


***Figure 72. Cumulative Failure for* LM124 Sequential HAST Exposure through 1100 Hours for Uncoated PDIPs, Coated PDIPs, and Hermetic DIP Controls.**

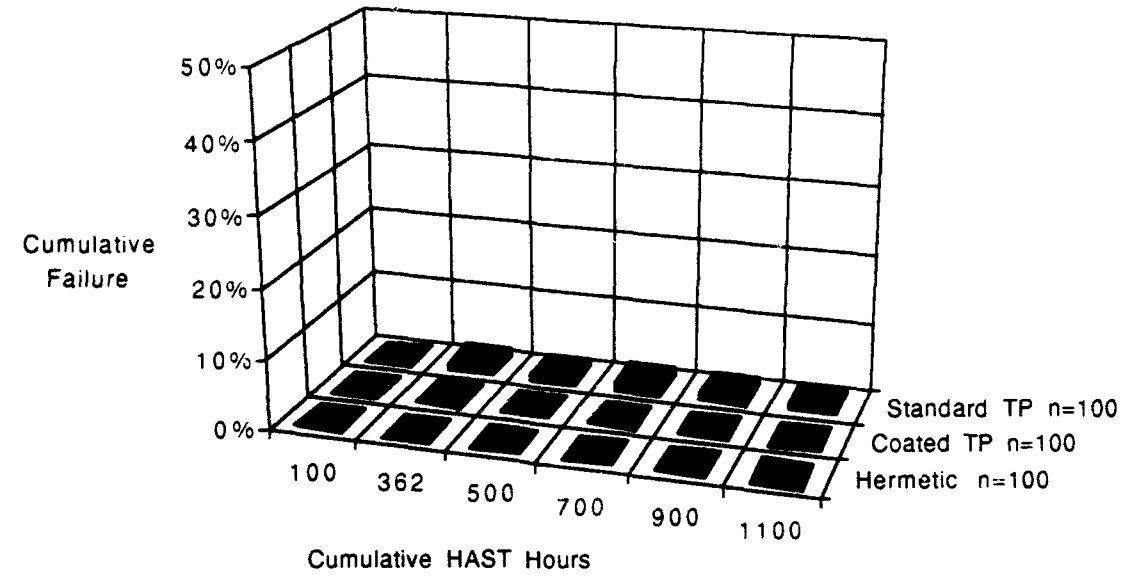


Figure 73. Cumulative Failure for LM124 Sequential HAST Exposure through 1100 Hours for Uncoated TapePak™, Coated TapePak™, and Hermetic DIP Controls.

Summary of LM124 Op-Amp Device Reliability

1. One failure was found through 1100 hours HAST exposure after preconditioning in the standard TapePak™ devices. This failure was determined to be corrosion of the field metal of the device related to moisture penetration through a small defect in the primary passivation of the device along a trace.

2. No failures were found through 1100 hours HAST exposure after preconditioning in the ceramic-coated TapePak™, standard PDIP, ceramic-coated PDIP, and hermetic DIP control devices.

3. Sequential HAST at 140°C for 1100 hours does not differentiate among LM124 standard and ceramic-coated TapePak™, standard and ceramic-coated PDIP, and hermetic DIP control devices.

4 Sequential HAST results for the LM124 at 140°C indicate that the low-temperature thin film ceramic die coating technology does not degrade the electrical performance of the IC in assembly or burn-in.

PROGRAM CONCLUSIONS

The objective of this program was to demonstrate the improved reliability of plastic packaged ICs using Dow Corning's Ceramic Coating Technology to provide a moisture/ion barrier on National Semiconductor's plastic encapsulated ICs. For this program, the assumption was made that certain facts would not invalidate the test.

- Plastic IC packages absorb moisture and will saturate in a relatively short time. This program does not attempt to provide or demonstrate a system of keeping moisture out of the epoxy molding compound, but rather provide a barrier to that moisture at the device/epoxy interface.

- Testing at temperatures above 125°C exceeds the maximum operating temperature of the IC and therefore may not reflect field operation conditions.

- HAST exposure at 159°C of the CD4011B approaches the glass transition temperature of the epoxy molding compounds used for plastic ICs.

Based on the work completed under this program, the following conclusions can be made:

1. Inorganic coated CMOS die in plastic packages surpasses the reliability of standard CMOS die by 600 hours to first failure in direct HAST exposure and approaches that of hermetic package reliability.

2. Weibull analysis of the plastic package reliability data reveals at least one order of magnitude decrease in failure rate was achieved through the use of protective inorganic coatings, applied prior to plastic encapsulation, as compared to standard plastic packages.

3. Low-temperature thin-film ceramic coatings do not degrade IC performance in assembly, burn-in, surface-mount assembly, or extended temperature cycling (-65 to 150°C), autoclave (121°C), and HAST (140°C, 159°C).

4. Device preconditioning, also referred to as sequential testing,

accelerates the time to failure by 100 hours in HAST exposure of plastic packaged CMOS devices.

5. Reliability differentiation in HAST at 159°C was achieved between ceramic-coated and standard commercial die in plastic packages. Protection of ICs from moisture and mobile ions using thin-film ceramics increased device lifetimes in sequential HAST exposure by 300 hours over standard plastic encapsulated ICs.

6. Reliability differentiation in HAST at 140°C was not achieved on LM124 TapePaK™ and PDIP test devices through 1100 hours.

7, Reliability differentiation in autoclave, HAST, and temperature cycling/salt fog exposures was consistently achieved between ceramic-coated and standard die in ceramic, sidebrazed, unlidded chip carriers with aluminum wire.

8. Ceramic-coated aluminum leadwires, unprotected from mechanical shock and vibration, are susceptible to fracture at the bondwire neckdown to frame regions of the chip carriers.

Future Directions

This study provides external validation of the significant improvement in reliability afforded by sealing a chip using Dow Corning's low-temperature inorganic coating (passivation) technology. The advancement of this technology to include wafer level application is proposed, which will provide the cost reduction improvements necessary to commercialize this technology. This will also provide a simplified packaging /passivation system for supplying sealed chips to the semiconductor industry. This enabling technology will facilitate the development of known-good-die (KGD) for advanced packaging applications, such as multichip modules, by providing sealed devices which are reliable over extended long-term storage and service life.

Acknowledgments

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Appendix A
Device Datasheets (LM124/CD4011)

National Semiconductor

May 1999

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

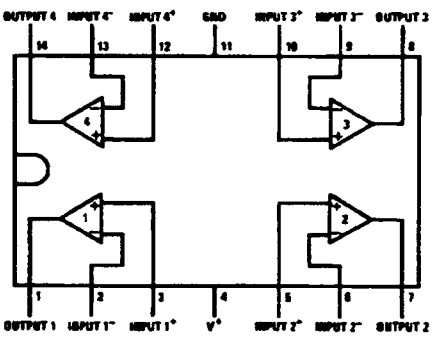
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3 V_{DC} to 32 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±16 V_{DC}
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package



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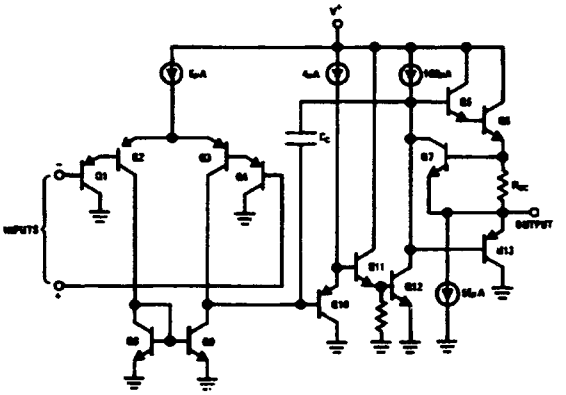
Top View

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N
See NS Package Number J14A, M14A or N14A

Schematic Diagram (Each Amplifier)



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}) (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics $V^+ = +5.0\ V_{DC}$, (Note 4), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5) $T_A = 25°C$		±1	±2		±1	±3		±2	±3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$		±2	±10		±2	±15		±5	±30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, (LM2902, $V^+ = 26\ V_{DC}$), $T_A = 25°C$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V_{DC}
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps																			mA_{DC}
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$, $R_L \geq 2\ k\Omega$, ($V_O = 1\ V_{DC}$ to $11\ V_{DC}$), $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5\ V_{DC}$, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	85		50	70		dB
Power Supply Rejection Ratio	DC, $V^+ = 5\ V_{DC}$ to $30\ V_{DC}$ (LM2902, $V^+ = 5\ V_{DC}$ to $26\ V_{DC}$), $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Amplifier-to-Amplifier Coupling (Note 8)		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
	Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 2\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
		$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_O = 200\ mV_{DC}$, $T_A = 25°C$	12	50		12	50		12	50		12	50		12	50		12	50		μA_{DC}
Short Circuit to Ground		(Note 2) $V^+ = 15\ V_{DC}$, $T_A = 25°C$		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage		(Note 5)			±4			±4			±5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift		$R_S = 0\Omega$		±7	±20		±7	±20		±7	±30		±7			±7			±7		$\mu V/°C$
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±30			±30			±75			±100			±150		±45	±200	nA_{DC}
Input Offset Current Drift		$R_S = 0\Omega$		±10	±200		±10	±200		±10	±200		±10			±10			±10		$pA_{DC}/°C$
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)		$V^+ = +30\ V_{DC}$ (LM2902, $V^+ = 26\ V_{DC}$)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain		$V^+ = +15\ V_{DC}$ (V_O Swing = 1 V_{DC} to 11 V_{DC}) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
		$R_L \geq 10\ k\Omega$ (LM2902, $V^+ = 26\ V_{DC}$)	27	28		27	28		27	28		27	28		27	28		23	24		
	V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \geq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}

Electrical Characteristics $V^+ = +5.0\ V_{DC}$ (Note 4) unless otherwise stated (Continued)

Parameter		Conditions		LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Current	Source	$V_O = 2\ V_{DC}$	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	Sink		$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15\ V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: *These specifications are limited to* $-55°C \le T_A \le +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \le T_A \le +70°C$, and the LM2902 specifications are limited to $-40°C \le T_A \le +85°C$.

Note 5: $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$; and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$) at 25°C; for LM2902, V^+ from $5\ V_{DC}$ to $26\ V_{DC}$

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32\ V_{DC}$ without damage ($+26\ V_{DC}$ for LM2902), independent of the magnitude of V^+.

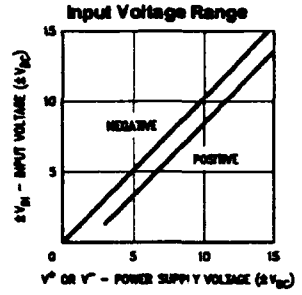
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

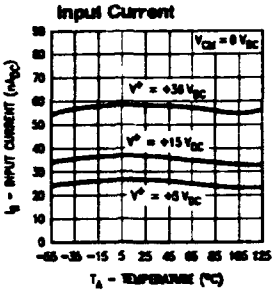
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

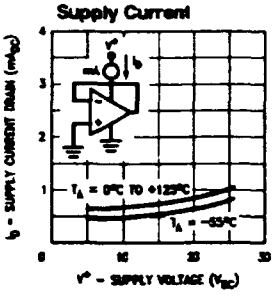
Input Voltage Range



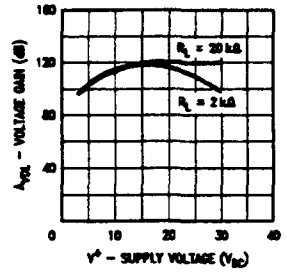
Input Current



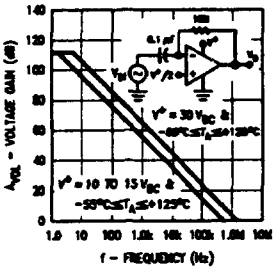
Supply Current



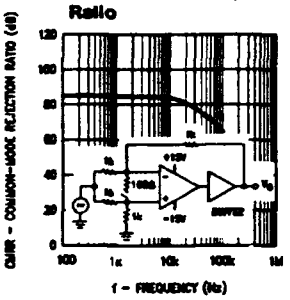
Voltage Gain



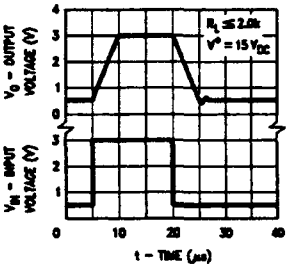
Open Loop Frequency Response



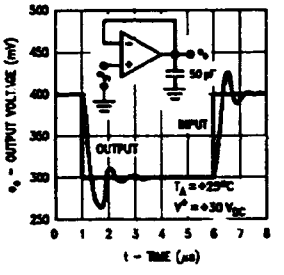
Common Mode Rejection Ratio



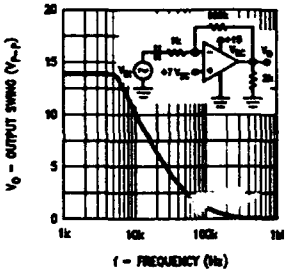
Voltage Follower Pulse Response



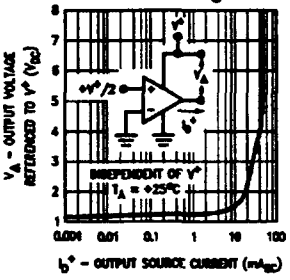
Voltage Follower Pulse Response (Small Signal)



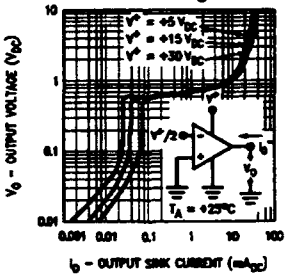
Large Signal Frequency Response



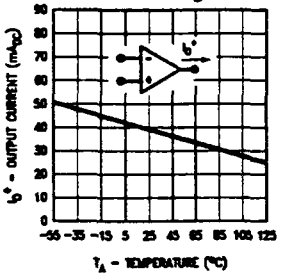
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



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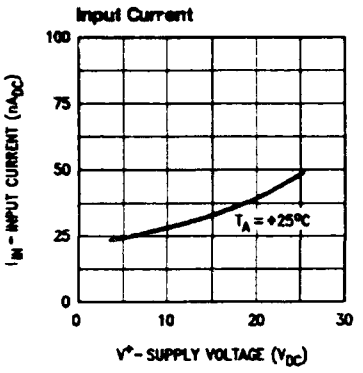
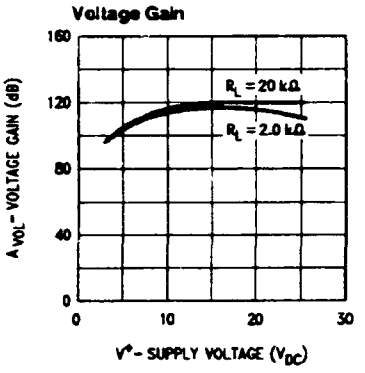
Typical Performance Characteristics (LM2902 only)





TL/H/9299–4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than -0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

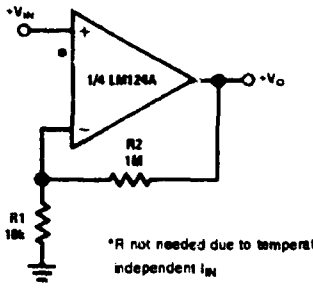
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

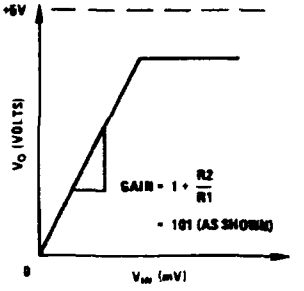
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

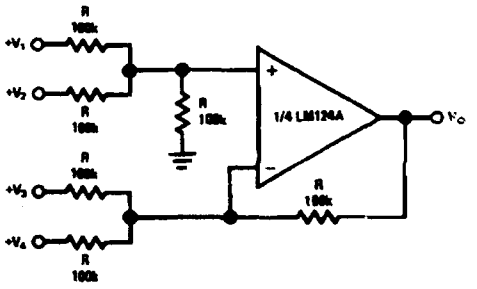
Non-Inverting DC Gain (0V Input = 0V Output)





TL/H/9299–5

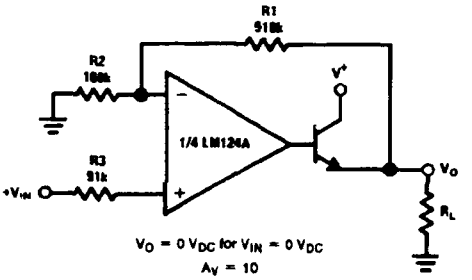
DC Summing Amplifier
(V_{IN}'s ≥ 0 V_{DC} and V_O ≥ V_{DC})



TL/H/9299–6

Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

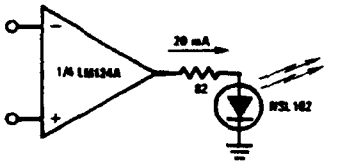
Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

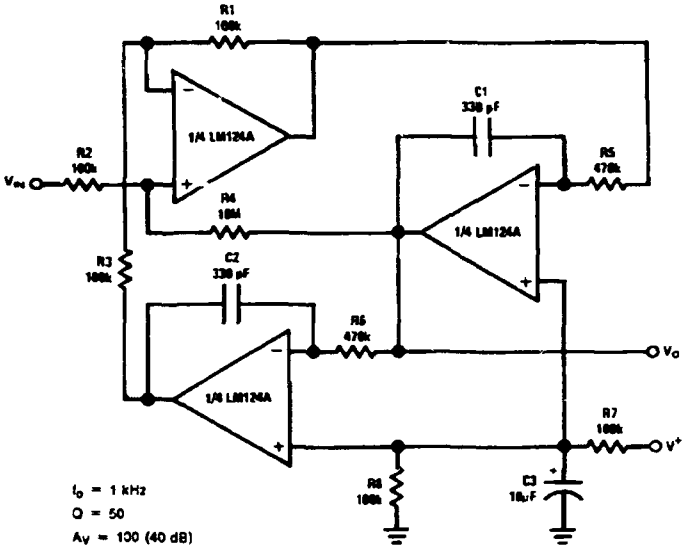
TL/H/9299–7

LED Driver



TL/H/9299–8

"BI-QUAD" RC Active Bandpass Filter

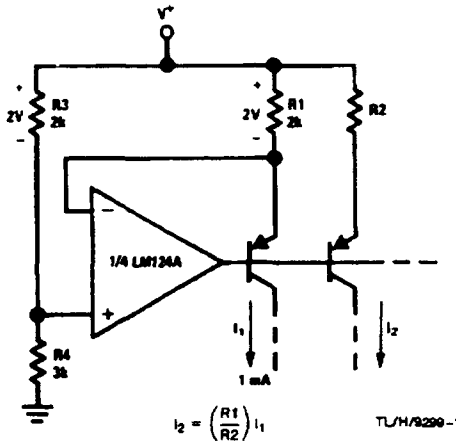


f_o = 1 kHz
Q = 50
A_V = 100 (40 dB)

TL/H/9299–9

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

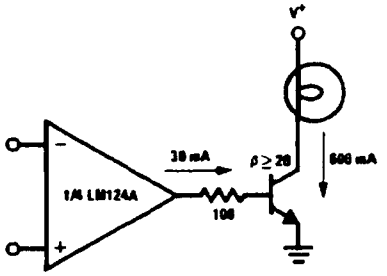
Fixed Current Sources



$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

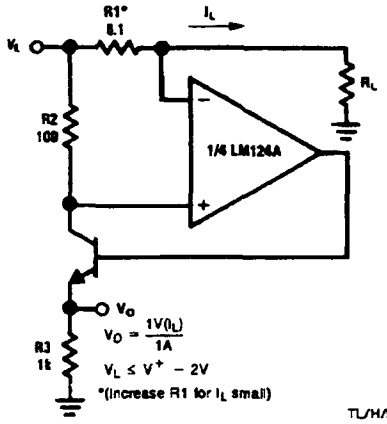
TL/H/9299–10

Lamp Driver



TL/H/9299–11

Current Monitor



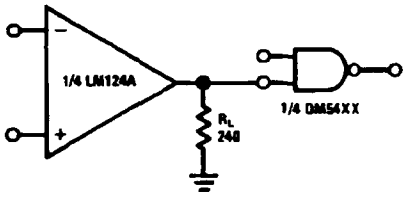
$$V_O = \frac{1V(I_L)}{1A}$$

$V_L \leq V^+ - 2V$

*(increase R1 for I_L small)

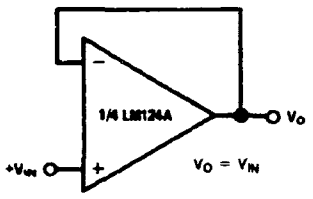
TL/H/9299–12

Driving TTL



TL/H/9299–13

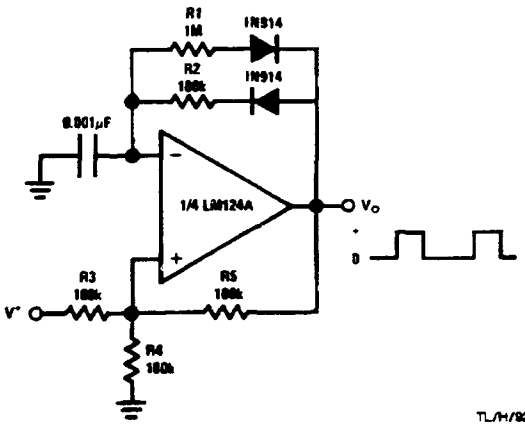
Voltage Follower



$V_O = V_{IN}$

TL/H/9299–14

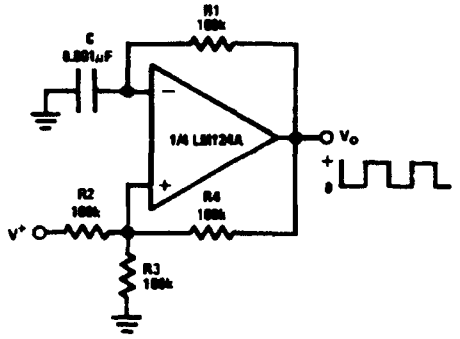
Pulse Generator



TL/H/9299–15

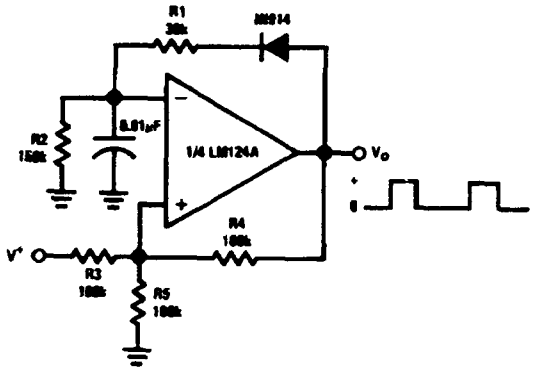
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Squarewave Oscillator



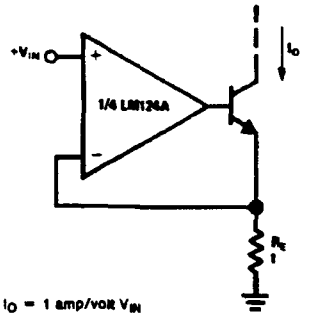
TL/H/9299–16

Pulse Generator



TL/H/9299–17

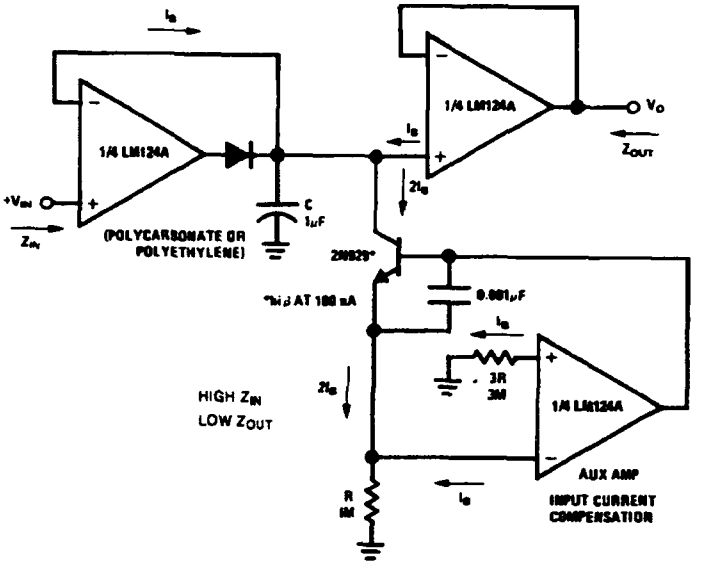
High Compliance Current Sink



I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

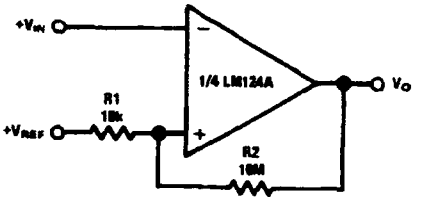
TL/H/9299–18

Low Drift Peak Detector



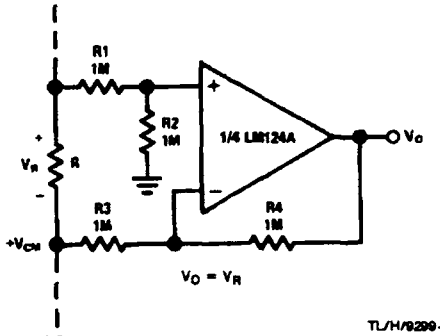
TL/H/9299–19

Comparator with Hysteresis



TL/H/9299–20

Ground Referencing a Differential Input Signal

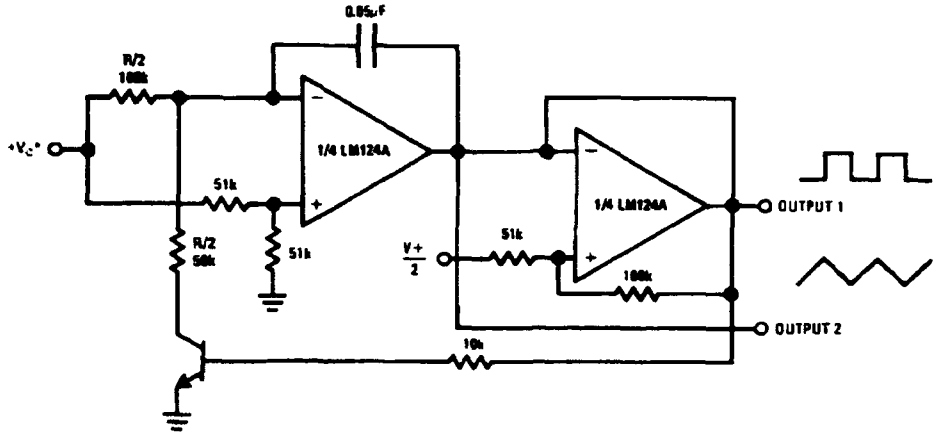


$V_O = V_R$

TL/H/9299–21

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

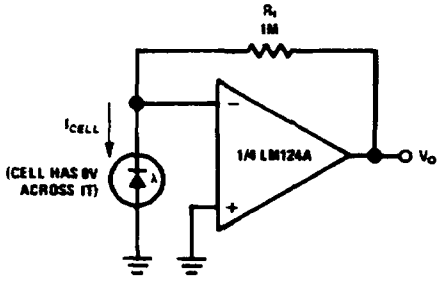
Voltage Controlled Oscillator Circuit



TL/H/9299–22

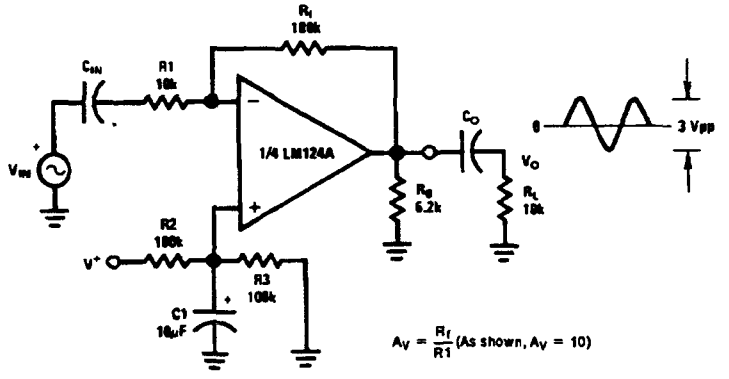
*Wide control voltage range: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5\ V_{DC})$

Photo Voltaic-Cell Amplifier



TL/H/9299–23

AC Coupled Inverting Amplifier

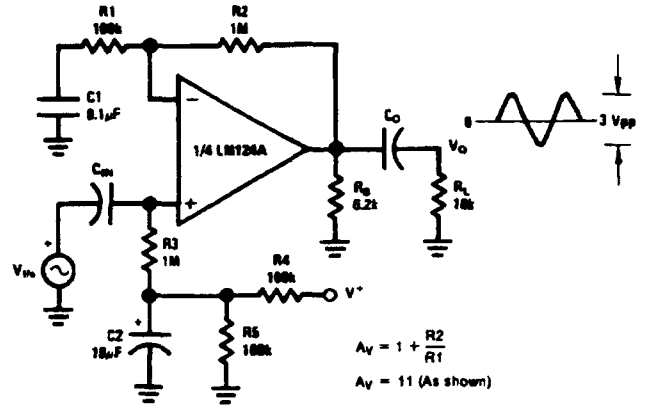


$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/9299–24

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier

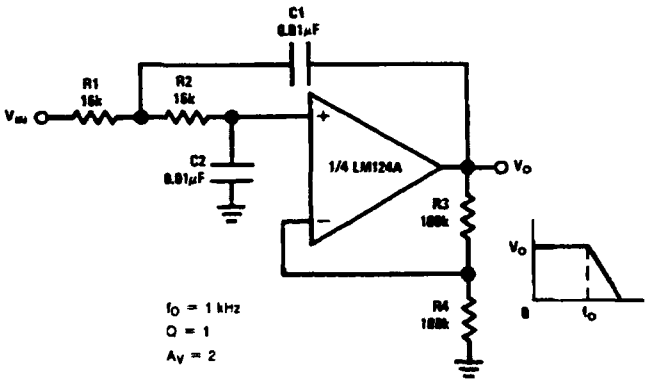


$A_V = 1 + \frac{R2}{R1}$

A_V = 11 (As shown)

TL/H/9299–25

DC Coupled Low-Pass RC Active Filter



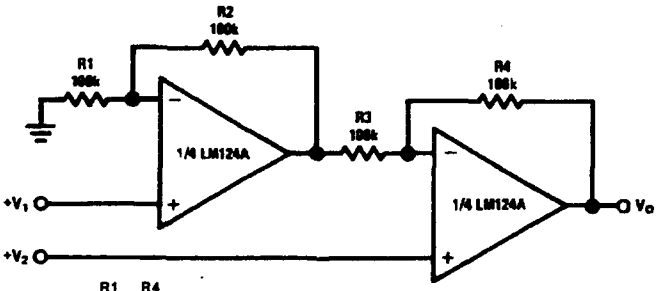
f_O = 1 kHz

Q = 1

A_V = 2

TL/H/9299–26

High Input Z, DC Differential Amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

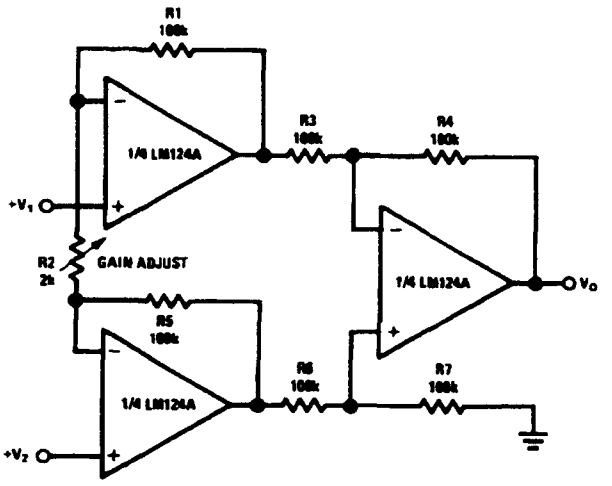
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

TL/H/9299–27

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier



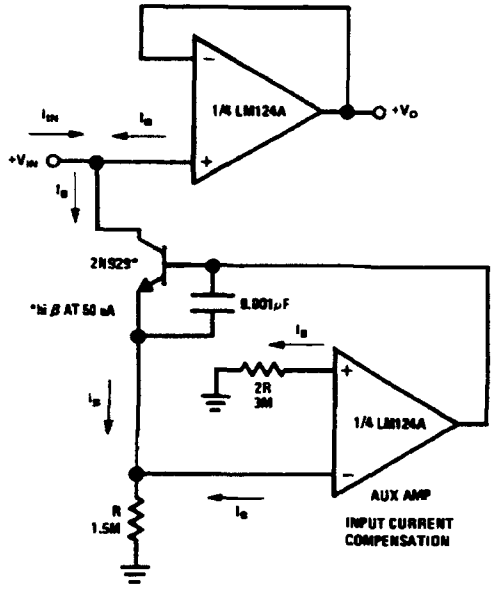
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

TL/H/9299–28

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

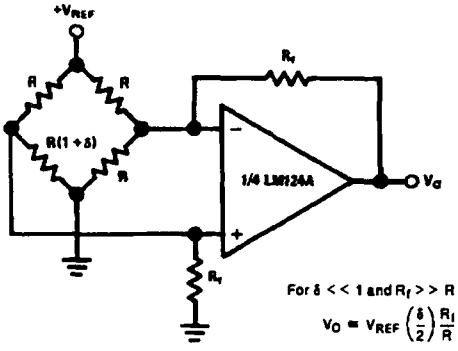
As shown $V_O = 101\ (V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/9299–29

Bridge Current Amplifier



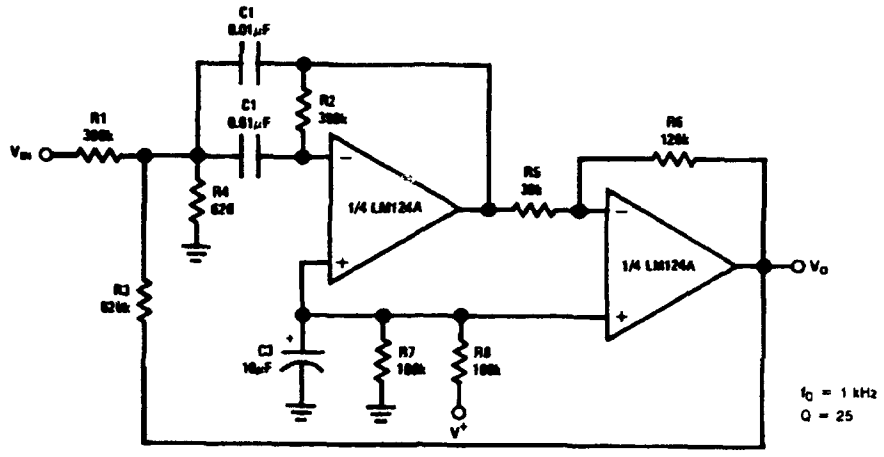
For $\delta << 1$ and $R_f >> R$

$$V_O = V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299–30

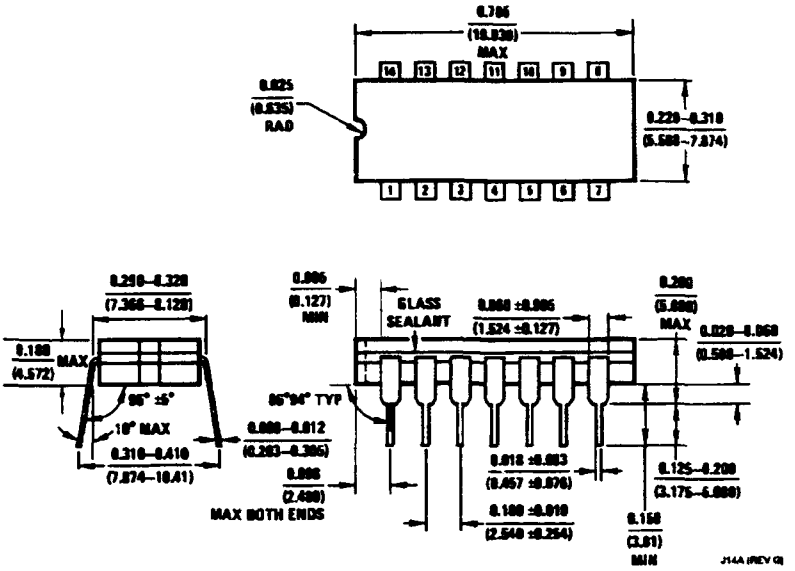
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Bandpass Active Filter

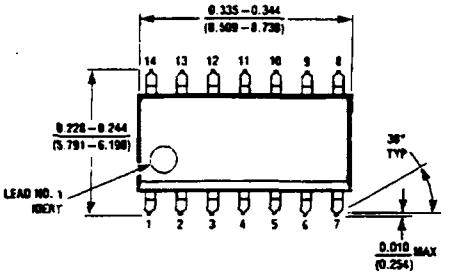


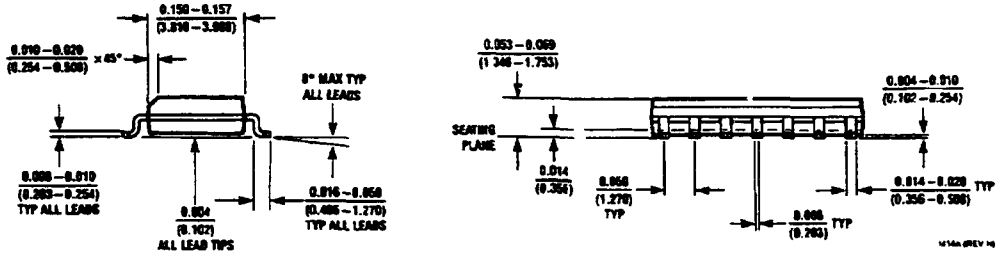
TL/H/8299–31

Physical Dimensions inches (millimeters)



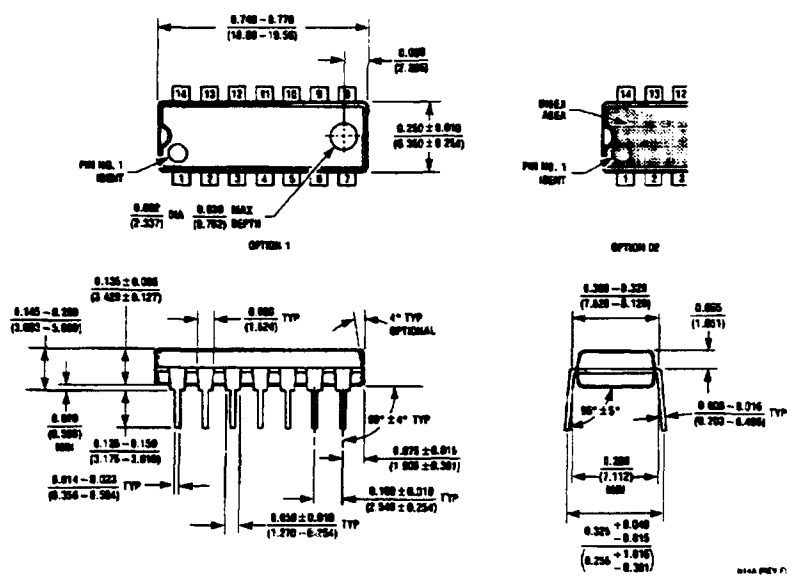
Ceramic Dual-In-Line Package (J)
Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J or LM324AJ
NS Package Number J14A





S.O. Package (M)
Order Number LM324M, LM324AM or LM2902M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order Number LM324N, LM324AN or LM2902N
NS Package Number N14A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

March 1988

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

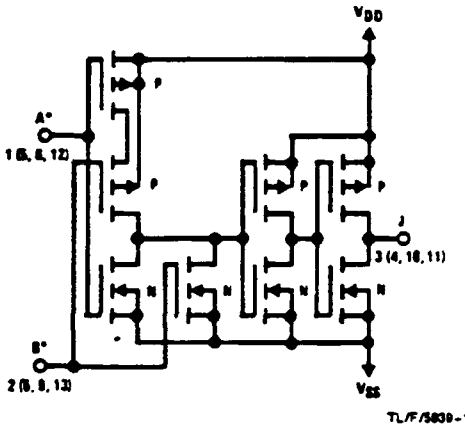
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

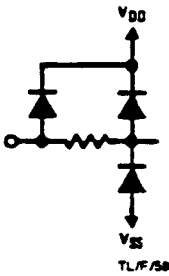
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Schematic Diagrams



TL/F/5839–1

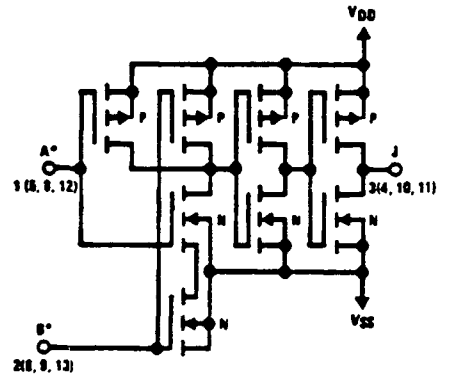
CD4001BC/BM



TL/F/5839–2

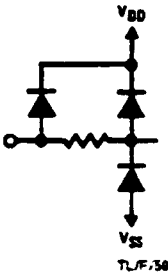
¼ of device shown
J = $\overline{A + B}$
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit



TL/F/5839–5

CD4011BC/BM



TL/F/5839–6

¼ of device shown
J = $\overline{A \cdot B}$
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

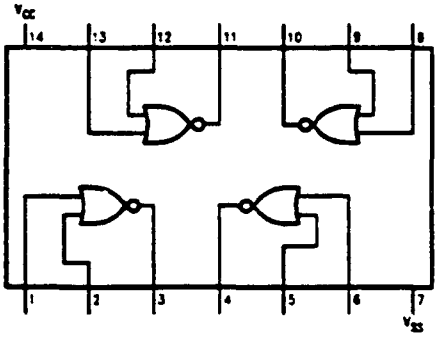
Operating Range (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range	
CD4001BM, CD4011BM	$-55°C$ to $+125°C$
CD4001BC, CD4011BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Connection Diagrams

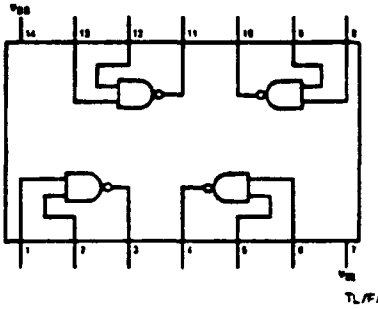
CD4001BC/CD4001BM
Dual-In-Line Package



TL/F/5939–3

Top View

CD4011BC/CD4011BM
Dual-In-Line Package



TL/F/5939–4

Top View

Order Number CD4001B or CD4011B

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics* CD4011BC, CD4011BM

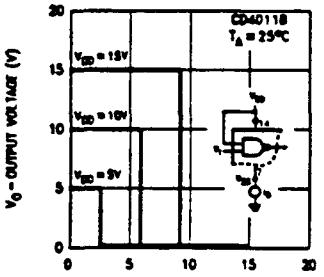
T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200k, Typical Temperature Coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

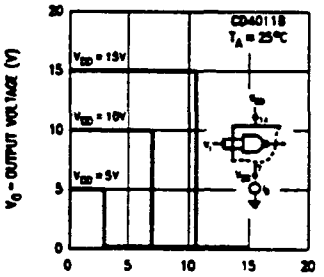
Typical Performance Characteristics

Typical Transfer Characteristics



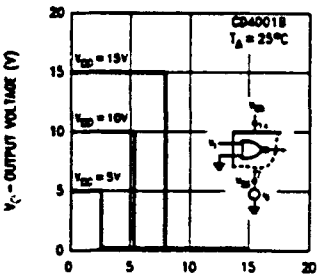
TL/F/5839–7

Typical Transfer Characteristics



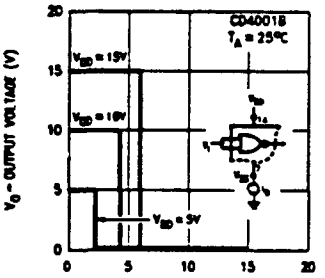
TL/F/5839–8

Typical Transfer Characteristics

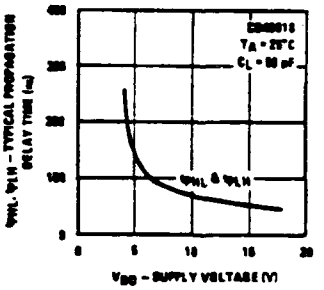


TL/F/5839–9

Typical Transfer Characteristics

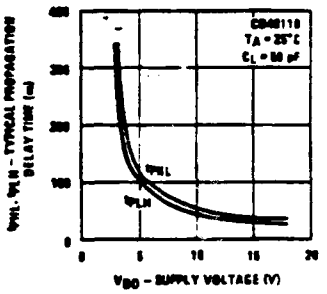


TL/F/5839–10



TL/F/5839–11

FIGURE 5



TL/F/5839–12

FIGURE 6

Typical Performance Characteristics (Continued)

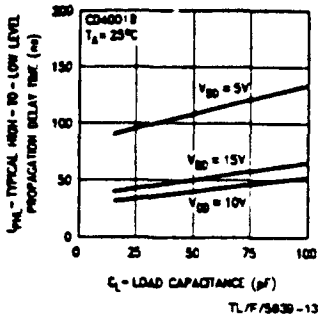


FIGURE 7

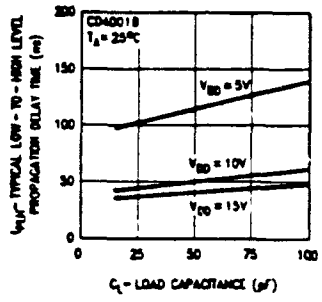


FIGURE 8

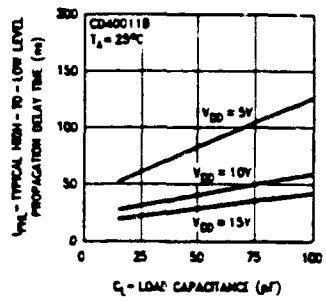


FIGURE 9

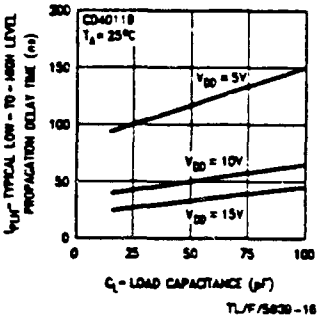


FIGURE 10

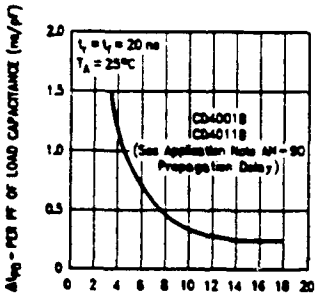


FIGURE 11

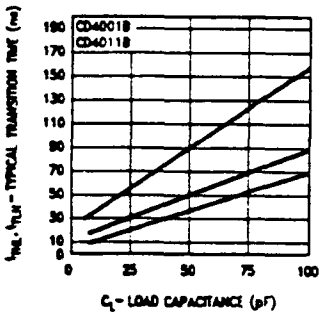


FIGURE 12

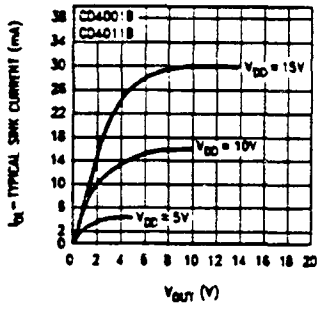


FIGURE 13

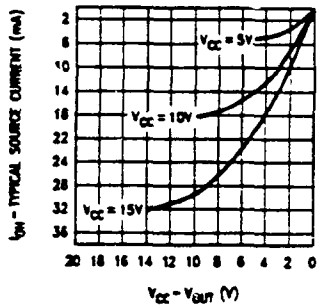
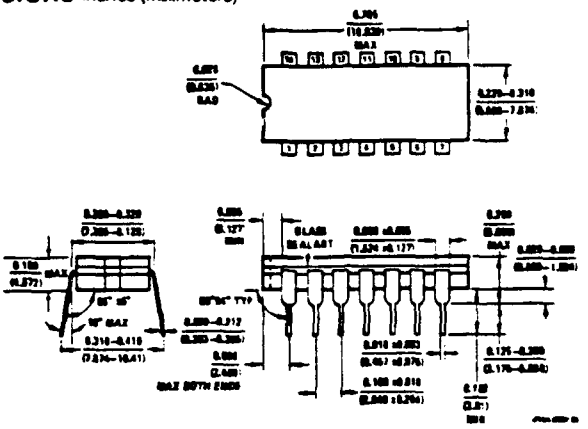
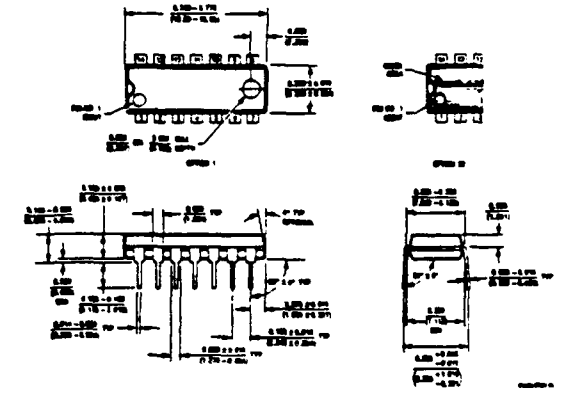


FIGURE 14

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4001BMJ, CD4001BCJ, CD40011BMJ or CD4011BCJ
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number CD4001BMN, CD4001BCN, CD4011BMN or CD4011BCN
NS Package Number N14A

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21/3 High Street
Bayswater, Victoria 3153
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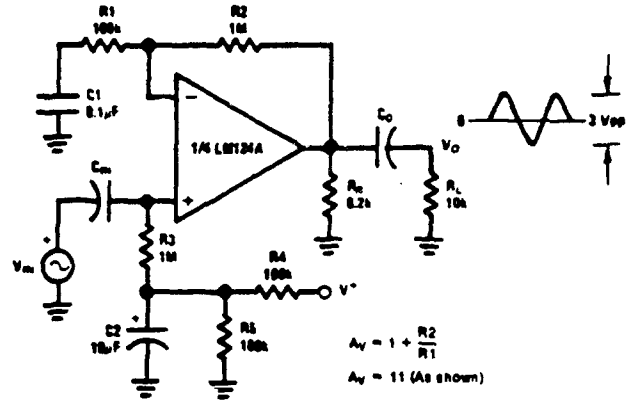
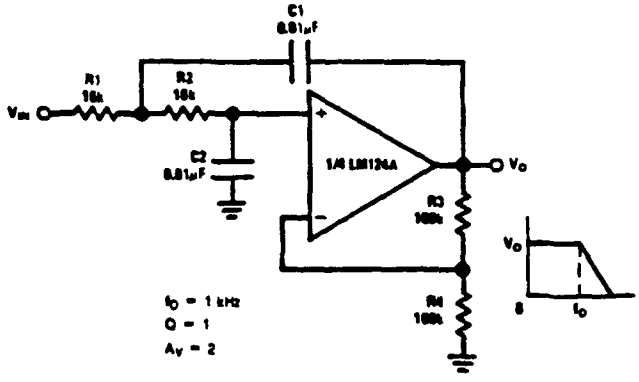
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

AC Coupled Non-Inverting Amplifier



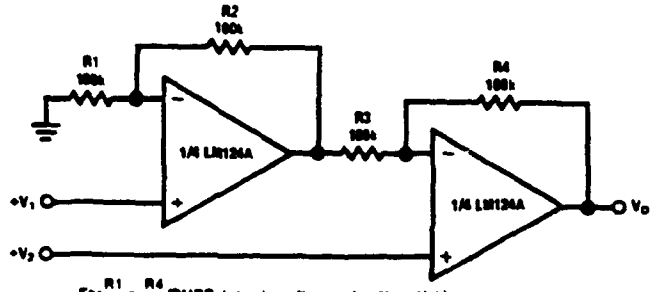
TL/H/8200–25

DC Coupled Low-Pass RC Active Filter



TL/H/8200–26

High Input Z, DC Differential Amplifier



For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

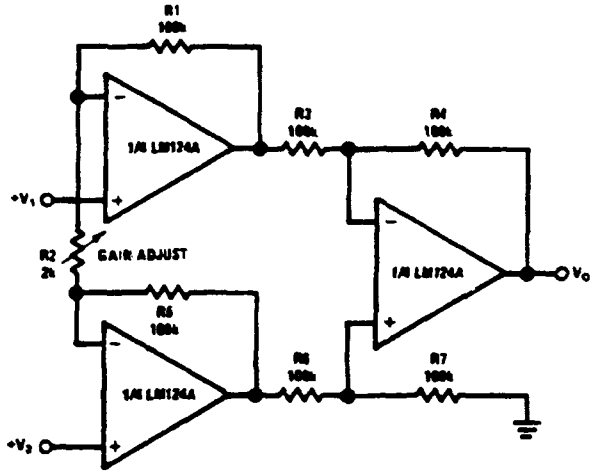
$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

TL/H/8200–27

Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

High Input Z Adjustable-Gain DC Instrumentation Amplifier



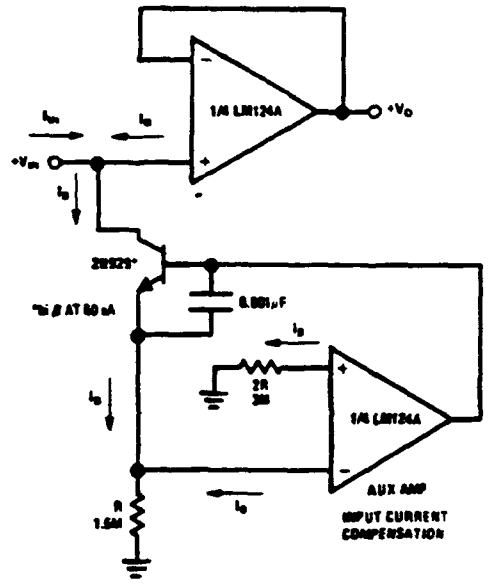
TL/H/5289–26

If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

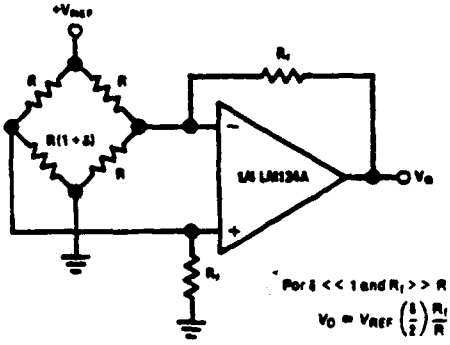
As shown $V_O = 101 (V_2 - V_1)$

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



TL/H/5289–29

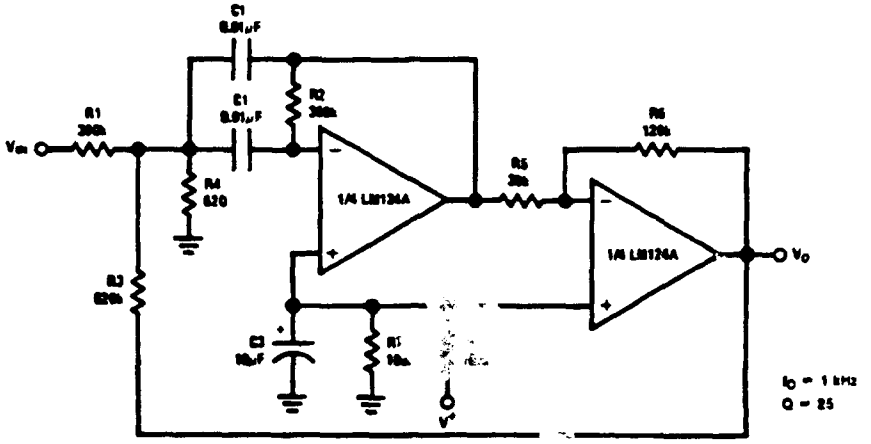
Bridge Current Amplifier



TL/H/5289–30

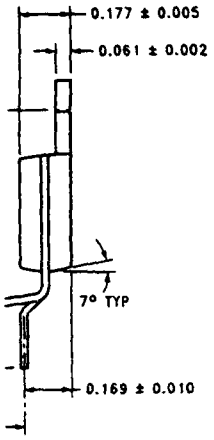
Typical Single-Supply Applications (V^+ = 5.0 V_{DC}) (Continued)

Bandpass Active Filter



TL/H/5890–31

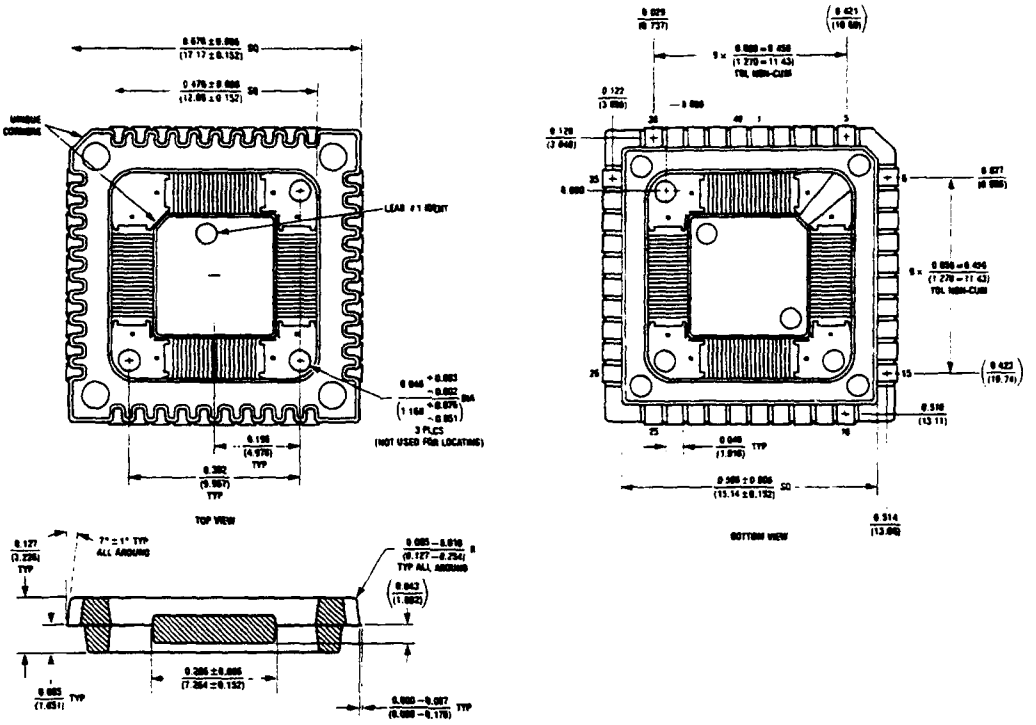
Appendix B
Package Drawings



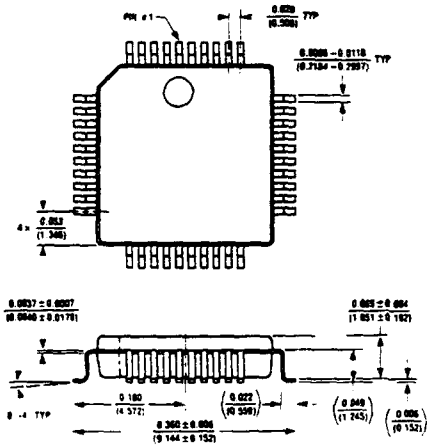
TA23A (REV A)

40 Lead Molded TapePak
NS Package Number TP40A

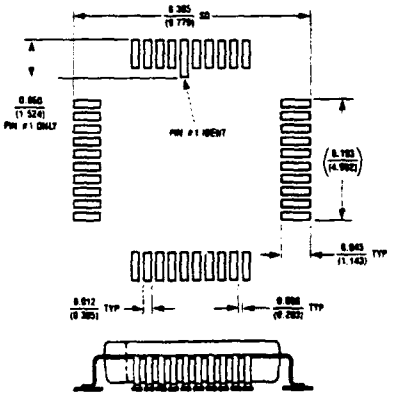
PACKAGE CONFIGURATION AS SHIPPED



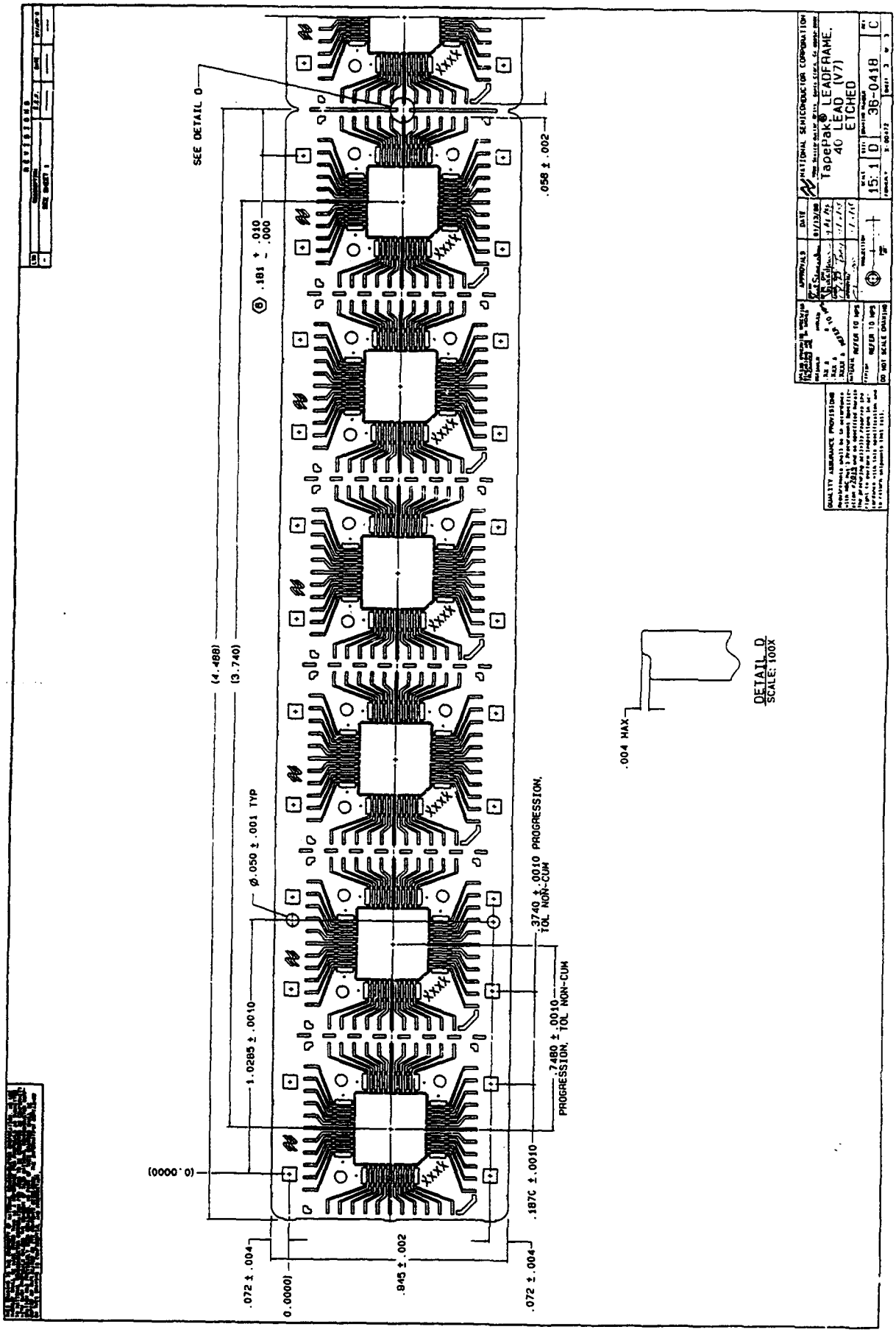
RECOMMENDED FORMED AND EXCISED PACKAGE OUTLINE

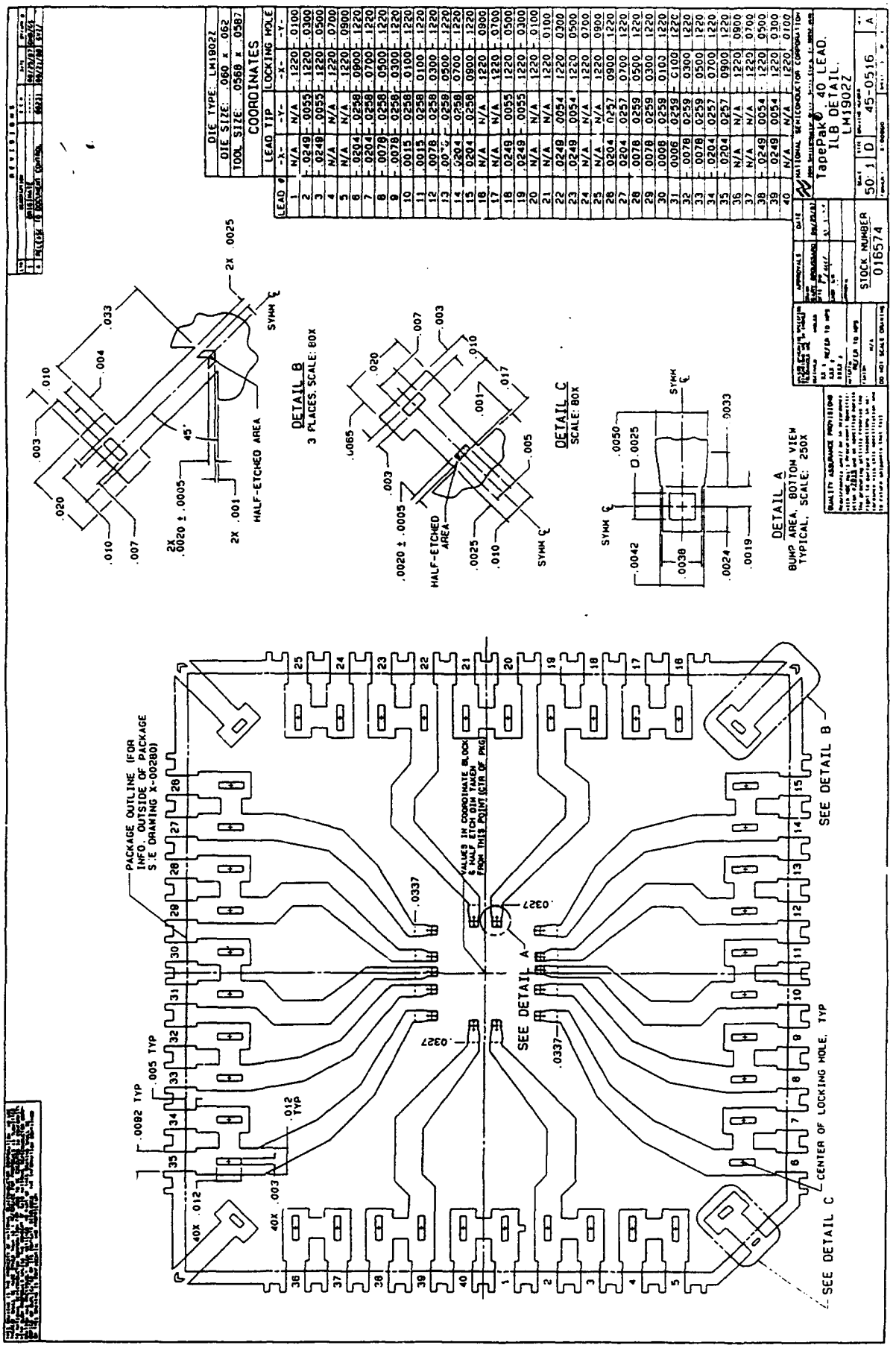


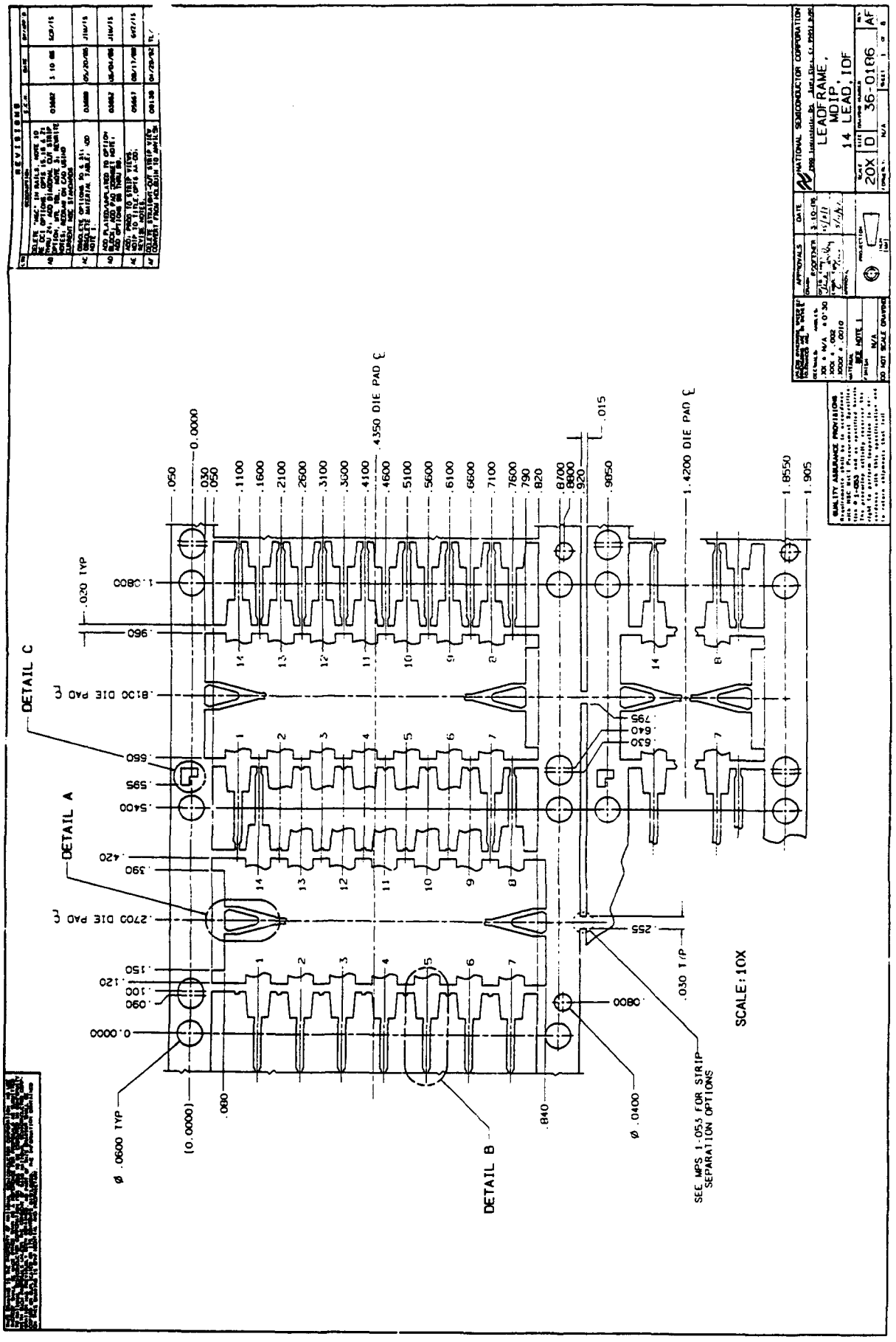
RECOMMENDED FOOTPRINT

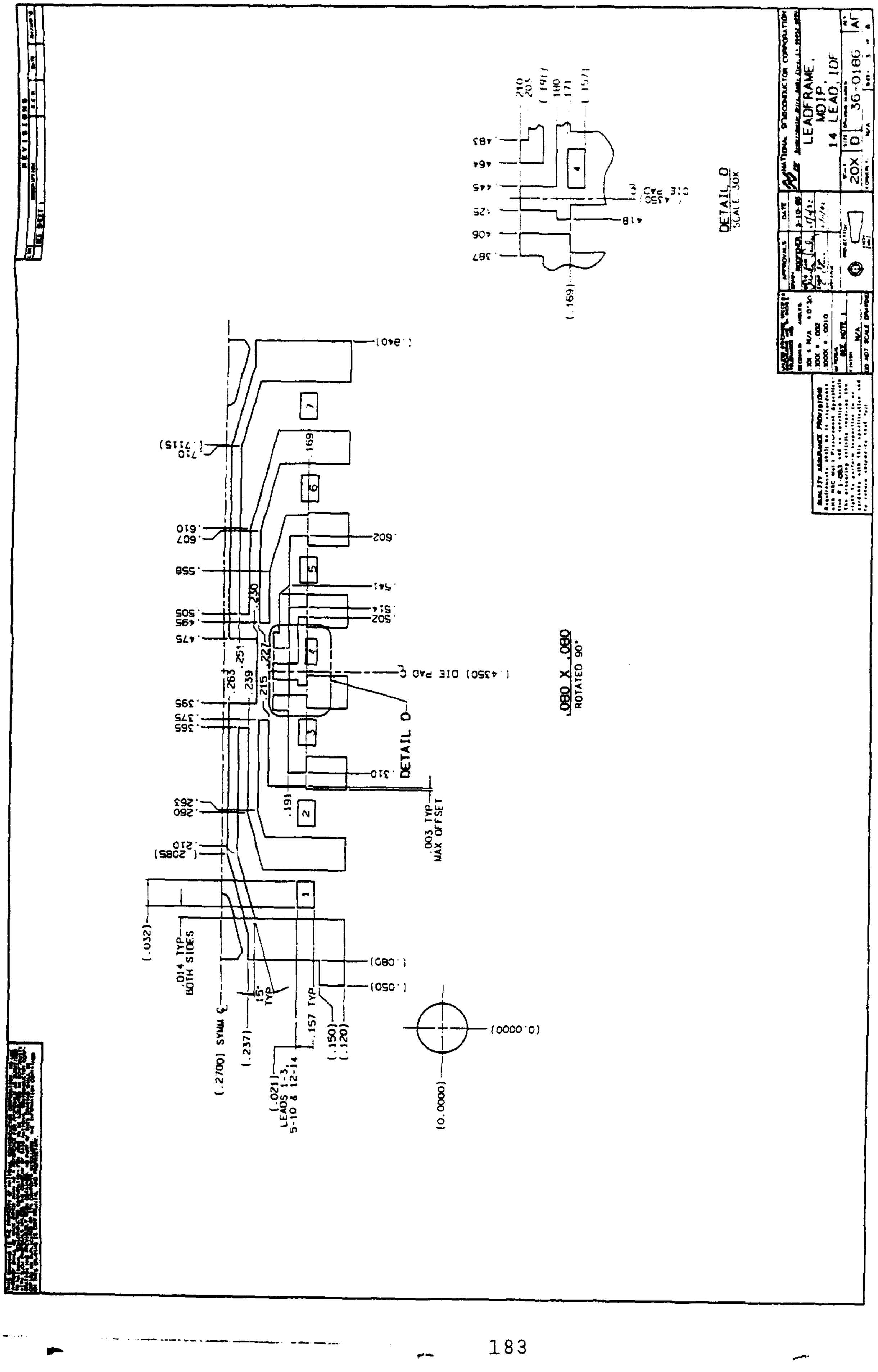


TP40A (REV A)


SEE DETAIL D
(4.488)
(3.740)
⑥ .181 +.010 -.000
.058 ±.002
Ø.050 ±.001 TYP
1.0285 ±.0010
.3740 ±.0010 PROGRESSION, TOL NON-CUM
.7480 ±.0010 PROGRESSION, TOL NON-CUM
(0000'.0)
.187C ±.0010
.072 ±.004
0.0000
.845 ±.002
.072 ±.004
.004 MAX
DETAIL D
SCALE: 100X
TapePak® LEADFRAME, 40 LEAD (V7) ETCHED
36-0418
C
15:1
D


DIE TYPE: LM19022
DIE SIZE: .060 x .062
TOOL SIZE: .0568 x .0587
COORDINATES
LEAD TIP
LOCKING HOLE
TapePak® 40 LEAD.
ILB DETAIL.
LM19022
STOCK NUMBER
016574
45-0516
DETAIL B
3 PLACES. SCALE: 80X
DETAIL C
SCALE: 80X
DETAIL A
BUMP AREA, BOTTOM VIEW
TYPICAL. SCALE: 250X
PACKAGE OUTLINE (FOR INFO, OUTSIDE OF PACKAGE S.E. DRAWING X-00280)
VALUES IN COORDINATE BLOCK & HALF ETCH DIM TAKEN FROM THIS POINT (CTR OF PKG)
SEE DETAIL A
SEE DETAIL B
SEE DETAIL C
CENTER OF LOCKING HOLE, TYP
HALF-ETCHED AREA
.0092 TYP
.005 TYP
.012 TYP


DETAIL C
DETAIL A
DETAIL B
SCALE: 10X
.020 TYP
.4350 DIE PAD ℄
1.4200 DIE PAD ℄
.8100 DIE PAD ℄
.2700 DIE PAD ℄
.030 T/P
Ø .0600 TYP
Ø .0400
SEE MPS 1-053 FOR STRIP SEPARATION OPTIONS
LEADFRAME, MDIP, 14 LEAD, 10F
NATIONAL SEMICONDUCTOR CORPORATION
20X
D
36-0186
AF


NATIONAL SEMICONDUCTOR CORPORATION
LEADFRAME, MDIP, 14 LEAD IDF
36-0186
20X
DETAIL D
SCALE 30X
.080 X .080
ROTATED 90°
(.4350) DIE PAD ℄
.003 TYP
MAX OFFSET
.014 TYP
BOTH SIDES
(.2700) SYMM ℄
(.021)
LEADS 1-3,
5-10 & 12-14
.157 TYP
(0.0000)
REVISIONS
QUALITY ASSURANCE PROVISIONS
DO NOT SCALE DRAWING

Appendix C

CD4011B Bond Pull Strength Data

Comparison Die (no die coat) on Leadframe

BOND PULL STRENGTH AND LOCATION RESULTS OF COATED CD4011 LEADFRAMES

BONDPULL STRENGTH

DESCRIPTION	UNIT NO	LEADWIRE NUMBER 1	2	3	4	5	6	7	8	9	10	11	12	13	14	AVG	MIN	MAX	STD
Unbonded Strip #5	3	16.3	15.5	16	14.3	13	14	13.3	14	13.8	13	10	10	13.5	11.3	13.39	10.00	14.00	1.76
	6	15	14	16.8	13.8	14.3	11.5	11.5	12.8	11.4	14.3	13	12.5	16.5	12	13.04	10.00	16.00	1.48
	9	14.5	13.3	13.3	12.3	15.8	14.5	11.3	15	15.4	16	15.5	11.8	12.5	13.3	13.97	11.30	16.00	1.67
	12	16.8	13.5	13	12.8	15	12.3	13	11.3	15	16.5	14.9	12.8	13	13.8	13.74	11.30	16.50	1.49
	AVG	15.33	14.69	14.83	13.33	14.83	13.69	12.88	13.69	14.39	14.79	13.37	11.78	12.46	12.10				
	MIN	14.00	13.30	13.80	12.30	13.80	11.80	11.30	11.30	11.80	13.80	10.00	10.00	10.80	11.30				
	MAX	16.80	15.80	16.80	14.30	15.80	14.80	13.30	15.80	16.80	16.80	15.80	12.80	13.80	12.80				
	STD	0.74	0.88	1.39	0.79	1.00	1.39	0.88	1.39	1.80	1.16	2.13	1.09	1.16	0.64				

LOCATION OF BREAK

3	2	2	3	2	2		2	2	4	2	4	2	2	2
6	2	4	2	2	4	2	2	4	4	2	2	2	2	2
9	2	4	2	2	3	2	4	2	2	4	2	2	2	2
12	3	4	2	2	2	2	2	2	3	3	2	2	2	

Experimental Ceramic Coated Die on Leadframe

BONDPULL STRENGTH DATA OF CERAMIC COATED LEADFRAMES

CD4011B 14-lead device, gold spot, 1.3 mil diameter gold wire; 6 coated devices per strip; Strip # 8.

***** STRIP 1 *****

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14	AVG	MIN	MAX	STD
1	14.0	12.0	12.5	12.5	12.0	13.5	12.0	13.0	10.5	13.0	10.5	12.0	12.0	11.5	12.21	10.50	14.00	0.98
2	11.0	11.0	11.0	10.5	12.0	11.5	11.5	15.0	13.0	14.0	12.0	11.5	11.0	11.5	11.89	10.50	15.00	1.23
3	13.0	14.0	12.0	12.0	11.0	13.0	10.5	0.0	13.0	12.0	13.0	13.0	14.5	12.0	12.07	0.00	14.50	1.97
4	14.5	12.5	14.0	13.0	12.0	13.5	12.0	10.5	14.0	15.0	14.5	12.5	12.0	12.5	13.04	10.50	15.00	1.22
5	12.5	12.0	11.0	13.0	13.0	11.5	12.0	9.5	13.5	11.5	14.0	11.0	11.5	12.5	12.04	9.50	14.00	1.13
6	11.5	12.0	13.5	10.0	11.5	12.0	11.0	13.0	12.0	11.5	13.0	12.0	13.5	13.0	12.11	10.00	13.50	0.97
7	13.5	12.0	13.0	13.5	11.5	10.5	11.5	12.0	11.0	14.5	10.5	13.0	13.0	14.0	12.39	10.50	14.50	1.34
8	12.5	13.0	13.0	9.0	11.5	10.0	11.0	12.0	13.0	13.0	13.0	13.0	11.5	14.5	12.14	9.00	14.50	1.38
AVG	12.81	12.31	12.50	11.69	11.81	11.94	11.44	11.38	12.69	13.06	12.56	12.25	12.38	12.69				
MIN	11.00	11.00	11.00	9.00	11.00	10.00	10.50	0.00	10.50	11.50	10.50	11.00	11.00	11.50				
MAX	14.50	14.00	14.00	13.50	13.00	13.50	12.00	15.00	14.00	15.00	14.50	13.50	14.00	14.50				
STD	1.12	0.85	1.03	1.54	0.66	1.24	0.53	2.66	1.15	1.39	1.36	0.71	1.11	1.03				

*** BREAK LOCATION ***

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	2	2	4	4	2	3	2	3	2	2	2	2	3	2
2	3	2	2	3	2	4	2	3	3	2	2	2	2	2
3	3	3	3	2	2	3	3	2	2	3	2	2	3	3
4	2	2	2	2	2	3	3	3	2	3	2	2	3	2
5	3	3	3	2	2	2	3	2	2	3	2	2	2	3
6	2	2	2	2	2	2	3	3	2	2	2	2	2	2
7	2	2	3	2	2	3	2	3	2	3	4	2	2	2
8	3	2	2	2	2	2	2	3	3	2	2	2	2	2

***** STRIP 2 *****

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14	AVG	MIN	MAX	STD
1	14.5	12.0	13.0	12.0	13.0	8.5	12.0	12.5	12.0	8.5	8.0	11.0	11.5	14.0	11.82	8.00	14.50	1.86
2	11.0	13.0	11.5	13.0	13.0	11.0	13.0	11.0	11.5	8.0	8.5	12.0	13.5	12.0	11.64	8.50	13.50	1.44
3	12.0	12.0	14.5	10.0	13.0	13.0	14.0	13.0	11.5	10.0	12.0	12.0	13.0	14.0	12.43	10.00	14.50	1.31
4	11.0	13.5	14.5	11.0	14.0	12.5	15.0	14.0	15.0	10.5	11.5	12.0	10.0	12.0	12.61	10.00	15.00	1.65
5	12.0	12.0	13.0	11.0	13.0	14.0	11.0	13.0	15.0	11.0	10.0	11.5	11.0	13.0	12.18	10.00	15.00	1.35
6	14.0	14.0	15.0	14.5	13.0	14.5	13.5	13.0	12.5	13.0	11.0	12.5	14.0	14.5	13.50	11.00	15.00	1.04
7	11.5	13.5	11.5	12.5	13.0	13.0	12.5	12.5	13.5	11.0	13.0	11.5	12.5	11.0	12.32	11.00	13.50	0.84
8	14.0	11.5	8.0	13.5	15.0	13.5	14.0	12.0	12.5	11.5	12.0	12.0	13.0	11.5	12.50	8.00	15.00	1.44
AVG	12.69	12.69	12.75	12.19	13.38	12.63	13.13	12.63	12.94	10.69	10.88	11.81	12.31	12.75				
MIN	11.00	11.50	8.00	10.00	13.00	8.50	11.00	11.00	11.50	8.00	8.50	11.00	10.00	11.00				
MAX	14.50	14.00	15.00	14.50	15.00	14.50	15.00	14.00	15.00	13.00	13.00	12.50	14.00	14.50				
STD	1.35	0.86	1.69	1.38	0.70	1.64	1.19	0.82	1.33	1.17	1.47	0.43	1.27	1.22				

*** BREAK LOCATION ***

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	3	2	2	2	2	2	2	2	2	2	2	2	2	3
2	2	2	4	3	2	2	2	2	2	2	2	2	2	2
3	2	2	2	2	4	3	3	4	2	2	2	2	2	2
4	2	2	2	2	3	3	2	3	2	2	2	2	3	2
5	2	2	2	2	2	2	2	2	3	2	2	2	2	2
6	3	2	2	2	2	3	3	2	2	2	2	2	3	3
7	2	2	2	2	2	2	2	2	2	2	2	2	2	2
8	2	2	3	2	2	3	2	2	2	2	2	2	2	2

***** STRIP 3 *****

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14	AVG	MIN	MAX	STD
1	14.0	15.0	14.5	14.0	13.0	14.0	13.0	14.5	14.5	13.5	12.0	14.0	12.0	13.0	13.64	12.00	15.00	0.89
2	13.0	14.0	16.0	12.0	12.5	16.0	14.0	14.0	14.0	11.5	13.0	12.0	14.0	13.5	12.88	10.00	14.00	1.37
3	13.0	15.0	15.5	16.0	11.0	12.0	13.0	11.5	14.0	13.5	13.0	13.0	14.5	12.5	12.61	10.00	15.00	1.42
4	13.0	13.0	12.5	12.5	12.0	12.5	12.0	13.0	12.5	12.5	11.5	14.0	13.0	12.0	12.57	11.50	14.00	0.89
5	14.0	13.5	8.0	11.0	15.0	12.5	13.5	14.0	13.0	12.0	11.5	15.0	14.5	13.5	13.00	8.00	15.00	1.91
6	13.0	15.0	12.5	11.0	13.5	12.0	13.0	11.5	12.0	11.0	12.0	13.5	11.5	14.0	12.54	11.00	15.00	1.14
7	12.5	13.0	12.5	11.5	11.5	12.0	13.0	11.5	12.0	12.5	13.0	13.5	14.5	12.5	12.54	11.50	14.50	0.91
8	12.0	14.0	14.0	12.0	11.5	12.5	13.0	10.0	13.0	11.0	14.5	14.5	15.0	12.5	12.82	10.00	15.00	1.41
AVG	13.06	14.06	11.94	11.75	12.50	12.19	13.06	12.5-	13.13	12.19	12.56	13.69	13.63	12.94				
MIN	12.00	13.00	8.00	10.00	11.00	10.00	12.00	10.0	12.00	11.00	11.50	12.00	11.50	12.00				
MAX	14.00	15.00	14.50	14.00	15.00	14.00	14.00	14.50	14.50	13.50	14.50	15.00	15.00	14.00				
STD	0.83	0.81	1.81	1.12	1.22	1.03	0.53	1.50	0.89	0.83	0.95	0.66	1.22	0.63				

*** BREAK LOCATION ***

UNIT #	LEADWIRE # 1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	4	2	3	3	2	2	3	3	2	3	2	2	3	4
2	3	4	2	2	2	3	3	3	2	2	2	3	3	2
3	3	2	2	2	2	2	2	2	2	2	2	2	2	2
4	4	3	2	2	2	2	2	2	2	2	3	2	3	3
5	2	2	2	2	2	3	3	2	2	2	2	2	3	3
6	2	3	2	2	2	3	2	2	2	2	2	2	3	3
7	4	3	3	2	2	2	2	2	2	2	3	2	3	2
8	2	2	2	2	2	3	2	2	3	2	2	2	3	2

Comparison Standard Die (Uncoated) in Open Cavity Packages

	Wire 1	Wire 2	Wire 3	Wire 4	Wire 5	Wire 6	Wire 7	Wire 8	Wire 9	Wire 10	Wire 11	Wire 12	Wire 13	Wire 14	AVG	MIN	MAX	STD
Device 1	12.5	9	11	12	11.5	11	13.5	8.5	8	10	12.5	10.5	11	11	10.86	8	13.5	1.57
Device 2	12.5	13.5	13.5	15.5	14.5	12.5	11.5	14	10.5	15	14.5	14	9	14.5	13.21	9	15.5	1.84
Device 3	12.5	8	10.5	13	10	10	10.5	10	9	10	12	9	11.5	10.5	10.46	8	13	1.39
Device 4	11	9.5	11	11	11.5	9	9	7	8	8	9.5	10	9.5	9	9.36	6	11.5	1.57
Device 5	10.5	9	11.5	11	11	9	9	10.5	9	9	12	10	11	9	10.11	9	12	1.10
Device 6	13	10.5	12.5	8	10	8	8	7	7.5	9.5	10.5	10	10.5	8.5	9.46	6	13	1.99
Device 7	12.5	7.5	13.5	12	11	8.5	9	6.5	7.5	11	12	11	8	12.5	10.18	6.5	13.5	2.28
Device 8	11.5	11	10	12.5	11	9	10	8	10	8.5	9.5	8	9	10.5	9.89	8	12.5	1.33
Device 9	9	9.5	14.5	14	10.5	10	12	10	9.5	10	11	9	10.5	10	10.68	9	14.5	1.71
Device 10	10.5	8	11	14.5	10.5	9	9.5	10.5	9.5	9	10.5	9.5	9.5	13	10.32	8	14.5	1.68
Device 11	11	8	11.5	11	11.5	9.5	10	10	9	11	10.5	11	9.5	11	10.18	8	11.5	1.44
Device 12	11.5	9	11	10	12.5	8	8	8	10.5	9	8	10	8	8	9.39	8	12.5	1.53
Device 13	15	9.5	10.5	12	10.5	7	7	7.5	7	7	11.5	10.5	10	10	9.64	7	15	2.37
Device 14	13	9	10.5	13.5	14	9	9.5	7	10	9	12	14.5	10	9	10.71	7	14.5	2.28
Device 15	14.5	8.5	11	10	12	9	8	8	7.5	7.5	8.5	15	9	8	9.75	7.5	15	2.49
Device 16	9.5	9.5	11	10.5	14.5	13.5	13.5	9.5	8.5	8	10	11	9	10	10.57	8	14.5	1.97
Device 17	11	8.5	10.5	11.5	14	9.5	10.5	7	8	8.5	10	14	9.5	10.5	10.21	7	14	2.03
Device 18	9	8.5	8.5	9.5	10.5	6	6	5.5	6	6.5	7.5	8.5	6.5	8.5	7.64	5.5	10.5	1.56
Device 19	10.5	9.5	14	8.5	13.5	8.5	9	10	8	9	10.5	9.5	9	8.5	9.86	8	14	1.81
Device 20	11	9	10	11	13	9	16	8	9.5	9	11	12	9	9	10.46	8	16	2.12
AVG	11.58	9.13	11.38	11.45	11.88	9.25	9.88	8.63	8.63	9.13	10.68	10.85	9.45	10.10				
MIN	9.00	6.00	8.50	8.00	10.00	6.00	6.00	5.50	6.00	6.00	7.50	8.00	6.50	8.00				
MAX	15.00	11.00	14.50	14.50	14.50	13.50	16.00	10.50	10.50	11.00	12.00	15.00	11.50	13.00				
STD	1.86	1.32	1.71	2.35	1.53	1.87	2.76	1.64	1.35	1.51	1.45	2.19	1.28	1.56				

	Leadwire 1	Leadwire 2	Leadwire 3	Leadwire 4	Leadwire 5	Leadwire 6	Leadwire 7	Leadwire 8	Leadwire 9	Leadwire 10	Leadwire 11	Leadwire 12	Leadwire 13	Leadwire 14
Device 1	2	2	2	2	2	4	4	2	2	2	2	2	2	2
Device 2	2	2	4	4	4	4	2	4	2	4	2	4	2	4
Device 3	2	1	2	2	2	2	2	2	2	2	2	2	2	2
Device 4	2	2	2	1	2	2	2	1	2	2	2	2	2	1
Device 5	1	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 6	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 7	1	1	2	1	2	2	2	2	2	2	2	2	2	2
Device 8	2	2	2	2	2	2	2	2	2	2	1	2	2	2
Device 9	2	2	4	2	2	2	4	2	2	2	2	2	2	2
Device 10	2	1	2	2	1	2	2	2	2	2	2	2	2	4
Device 11	2	1	2	1	2	2	4	1	1	2	2	2	2	2
Device 12	2	2	2	2	2	2	2	2	2	2	1	2	2	2
Device 13	4	2	2	2	2	2	2	2	2	2	4	2	2	1
Device 14	2	2	2	4	2	2	2	2	2	2	2	4	2	2
Device 15	2	2	2	2	2	2	2	2	2	2	2	4	2	2
Device 16	2	2	2	4	4	4	2	2	2	2	2	2	2	2
Device 17	2	2	2	1	2	2	2	2	2	2	2	2	2	2
Device 18	2	2	2	2	2	2	2	2	2	2	1	2	2	2
Device 19	2	2	4	2	2	2	2	4	2	2	2	2	2	2
Device 20	2	2	2	2	2	2	2	4	2	2	2	2	2	2

Experimental Ceramic Coated Die in Open Cavity Packages

	Wire 1	Wire 2	Wire 3	Wire 4	Wire 5	Wire 6	Wire 7	Wire 8	Wire 9	Wire 10	Wire 11	Wire 12	Wire 13	Wire 14	AVG	MIN	MAX	STD
Device 1	4.5	5	5.5	10	8.5	9.5	6	6	6	5	4.5	5.5	5.5	5	6.18	4.5	10	1.80
Device 2	5.5	5.5	5	6.5	6	6	6	5.5	7.5	5.5	7.5	5	4.5	4.5	5.75	4.5	7.5	0.94
Device 3	5.5	5.5	5.5	9	10	6	6.5	6	6	6.5	9.5	6	5	5.5	6.61	5	10	1.63
Device 4	5	5	6	6.5	8	6	7	7.5	8.5	6	7	6.5	5	5.5	6.39	5	8.5	1.11
Device 5	6	4.5	6	6.5	7.5	6.5	7.5	8.5	6	7	6	6.5	5	5	6.46	4.5	8.5	1.17
Device 6	5.5	5	6	6.5	8	5	5.5	5	5.5	5	5.5	5.5	4.5	4.5	5.64	4.5	8.5	1.18
Device 7	5.5	5.5	6	7.5	6	5.5	7	7	5.5	7	7.5	6	5	5.5	6.18	5	7.5	0.85
Device 8	6.5	5	6	7.5	8	5.5	5	5.5	5	5	5.5	5.5	5	6	5.79	5	8	0.96
Device 9	5.5	5	6	6	8.5	6	6.5	6	6	6.5	8	5.5	4	6	6.11	4	8.5	1.11
Device 10	5	6.5	5	6.5	8.5	5	5	6	6	6.5	7	6.5	6	6.5	6.14	5	8.5	0.97
Device 11	6.5	5	5.5	7	5.5	4	5.5	5.5	5.5	5.5	7.5	5	4.5	4.5	5.50	4	7.5	0.96
Device 12	5	5	4.5	7.5	5.5	5.5	6.5	6.5	5	5.5	6.5	5	4.5	5	5.54	4.5	7.5	0.89
Device 13	4.5	5	6	7.5	9.5	5.5	6	5.5	6	5	6.5	5.5	5	5	5.89	4.5	9.5	1.29
Device 14	6	5.5	6	7	6	5.5	6	6	6	5.5	6	5	5.5	5	5.79	5	7	0.51
Device 15	5	5	5.5	7	6	5.5	6	6	5	5.5	7.5	5	4.5	4.5	5.57	4.5	7.5	0.87
Device 16	5	5.5	6	9	8.5	6	7	6.5	5	6.5	5.5	4.5	5	5.5	6.11	4.5	9	1.32
Device 17	6	5.5	6	7	7	6.5	6	6.5	7	6	8	6.5	4.5	6	6.32	4.5	8	0.82
Device 18	5	5	6	7	7	6	6.5	5	6.5	6	7.5	6.5	5	6	6.07	5	7.5	0.83
Device 19	5.5	6	6	7.5	5	5	4.5	5.5	5	5.5	7	6	5.5	5.5	5.86	4.5	7.5	0.80
Device 20	6.5	6	5.5	8	6	4	4.5	5.5	4.5	5	5	5.5	5	5.5	5.46	4	8	0.99
AVG	5.58	5.30	5.70	7.55	7.15	5.83	6.03	5.88	5.88	5.80	6.75	5.65	4.93	5.33				
MIN	4.50	4.50	4.50	6.00	5.00	4.00	4.50	5.00	4.50	5.00	5.00	4.50	4.00	4.50				
MAX	8.00	6.50	6.00	9.00	10.00	8.00	7.50	7.50	8.50	7.00	9.50	6.50	6.00	6.50				
STD	0.99	0.57	0.50	0.67	1.48	1.09	0.96	0.75	1.11	0.71	1.15	0.69	0.54	0.64				

	Leadwire 1	Leadwire 2	Leadwire 3	Leadwire 4	Leadwire 5	Leadwire 6	Leadwire 7	Leadwire 8	Leadwire 9	Leadwire 10	Leadwire 11	Leadwire 12	Leadwire 13	Leadwire 14
Device 1	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 2	2	2	2	2	2	2	2	2	4	2	2	2	2	2
Device 3	2	2	2	2	2	2	2	2	2	2	4	2	2	2
Device 4	2	2	2	2	2	4	2	2	4	2	2	2	2	2
Device 5	2	2	2	2	2	2	2	2	4	2	4	2	2	3
Device 6	2	2	2	2	2	2	3	2	4	2	2	2	2	2
Device 7	2	2	2	2	2	2	2	2	3	2	2	2	2	2
Device 8	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 9	2	2	2	2	4	4	2	2	2	2	2	2	2	2
Device 10	2	2	2	2	2	2	2	2	2	2	2	2	2	3
Device 11	4	2	2	2	2	2	4	2	2	4	2	2	2	2
Device 12	2	2	2	2	2	2	2	2	2	4	2	2	2	2
Device 13	2	2	2	2	2	2	2	2	2	2	4	2	2	2
Device 14	2	2	4	2	2	2	2	2	2	2	2	2	2	2
Device 15	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 16	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 17	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 18	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 19	2	2	2	2	2	2	2	2	2	2	2	2	2	2
Device 20	3	2	2	2	2	2	2	3	2	2	2	2	2	2

Appendix D

Electrical Test Parameters

```
Device:  01      INITIAL          CD4011B
Date & Time: Thu 04-08-93 @ 15:17:29.62
Diode Tests: (Pass)
Functional Test at  3  volts (Pass)
Functional Test at  18  volts (Pass)
Quescent Current (IL): VDD = 5 volts (( .000001  amp)
  Inputs Low:  0 (Pass)                    Inputs High:  1.2207E-09 (Pass)
Quescent Current (IL): VDD = 15 volts (( .000004  amp)
  Inputs High:  6.10352E-09 (Pass)       Inputs Low:  1.2207E-08 (Pass)
Input Current: VDD = 15 volts (-3E-07 (ILL( 3E-07  amp)
  Pin 1    IIL =  1.2207E-09 (Pass)    IIH =  1.2207E-09 (Pass)
  Pin 5    IIL =  1.2207E-09 (Pass)    IIH =  1.2207E-09 (Pass)
  Pin 9    IIL =  1.2207E-09 (Pass)    IIH =  1.2207E-09 (Pass)
  Pin 13   IIL =  6.10352E-10 (Pass)    IIH =  1.2207E-09 (Pass)
  Pin 2    IIH =  1.2207E-09 (Pass)    IIL =  6.10352E-10 (Pass)
  Pin 6    IIL =  0 (Pass)    IIH =  1.2207E-09 (Pass)
  Pin 8    IIH =  1.2207E-09 (Pass)    IIL =  6.10352E-10 (Pass)
  Pin 12   IIL =  0 (Pass)    IIH =  1.2207E-09 (Pass)
Output Current Drive
  IOH(5v) ()-.00044 ) amp:
    Pin( 3 ) = -9.1732E-04 (Pass)     Pin( 4 ) = -9.1259E-04 (Pass)
    Pin( 10 ) = -9.09729E-04 (Pass)     Pin( 11 ) = -9.10912E-04 (Pass)
  IOL(5v) () .00044 ) amp:
    Pin( 3 ) =  8.13675E-04 (Pass)     Pin( 4 ) =  8.10776E-04 (Pass)
    Pin( 10 ) =  8.22868E-04 (Pass)     Pin( 11 ) =  8.29163E-04 (Pass)
  IOL(15v) () .003 ) amp:
    Pin( 3 ) =  8.67386E-03 (Pass)     Pin( 4 ) =  8.62083E-03 (Pass)
    Pin( 10 ) =  8.85773E-03 (Pass)     Pin( 11 ) =  8.89244E-03 (Pass)
  IOH(15v) ()-.003 ) amp:
    Pin( 3 ) = -7.71828E-03 (Pass)     Pin( 4 ) = -7.61719E-03 (Pass)
    Pin( 10 ) = -7.56226E-03 (Pass)     Pin( 11 ) = -7.70073E-03 (Pass)
Voltage Output
  VOH() 4.95498 ) @ VDD =  5.00498  volts:
    Pin( 3 ) =  5.00641 (Pass)     Pin( 4 ) =  5.0061 (Pass)
    Pin( 10 ) =  5.00641 (Pass)     Pin( 11 ) =  5.00641 (Pass)
  VOL(( .05 ) @ VDD =  5.00498  volts:
    Pin( 3 ) =  0 (Pass)     Pin( 4 ) = -1.00677E-04 (Pass)
    Pin( 10 ) = -1.52541E-05 (Pass)     Pin( 11 ) = -9.15248E-06 (Pass)
  VOL(( .05 ) @ VDD =  15.0073  volts:
    Pin( 3 ) = -1.22033E-05 (Pass)     Pin( 4 ) =  0 (Pass)
    Pin( 10 ) = -3.05083E-05 (Pass)     Pin( 11 ) =  3.05083E-06 (Pass)
  VOH() 14.9573 ) @ VDD =  15.0073  volts:
    Pin( 3 ) =  15.0122 (Pass)     Pin( 4 ) =  15.0134 (Pass)
    Pin( 10 ) =  15.0134 (Pass)     Pin( 11 ) =  15.0122 (Pass)
Voltage Input Switch Points: @ VDD=5v (1.5 v ( VI ( 3.5 v)
  Rising Input: .02 volt Steps (Pass)
    Pin(3) =  2.96  volts          Pin(4) =  2.96  volts
    Pin(10) =  2.96  volts          Pin(11) =  2.96  volts
Voltage Input Switch Points: @ VDD=15v (4 v ( VI ( 11 v)
  Rising Input: .02 volt Steps (Pass)
    Pin(3) =  7.96  volts          Pin(4) =  8.08  volts
    Pin(10) =  7.98  volts          Pin(11) =  8.1  volts
01 Passed All Tests
```

NOTES	RETS124AX REVISION 9A		TEST CONDITION UNLESS OTHERWISE SPECIFIED All voltages referenced to device ground.			TEST SYSTEM: DC PARAMETERS						DRIFT LIMITS	UNITS
						SBGRP 1		SBGRP 2		SBGRP 3			
						25 C		125 C		-55 C			
	PARAMETER	SYM	V+		TEST #	min	max	min	max	min	max	25 C	
	Power Supply Current	Icc	5V				1.2		1.2		1.2		mA
			30V				3.0		4.0		4.0		mA
	Output Sink Current	Isink	15V	Vout = 200 mV		12							uA
			15V	Vout = 2V		10		5		5			mA
	Output Source Current	Isource	15V	Vout = 2V			-20		-10		-10		mA
	Short Circuit Current	Ios	5V	Vout = 0V		-60							mA
6	Input Offset Voltage	Vio	30V	Vcm = 0V		-2	2	-4	4	-4	4		mV
			30V	Vcm = 28V		-2	2	-4	4	-4	4		mV
			5V	Vcm = 0V		-2	2	-4	4	-4	4		mV
	Common Mode Rejection Ratio	CMRR	30V	Vin = 0V to 28.5V		70							dB
	Input Bias Current	+Iib	5V	Vcm = 0V		-50	10	-100	10	-100	10		nA
		-Iib	5V	Vcm = 0V		-50	10	-100	10	-100	10		nA
	Input Offset Current	Iio	5V	Vcm = 0V		-10	10	-30	30	-30	30		nA
	Power Supply Rejection Ratio	PSRR		V+ = 5V to 30V, Vcm = 0V		65							dB
1	Common Mode Voltage	Vcm	30V				28.5		28		28		V

NOTE 1: Parameter tested go-no-go only.
NOTE 6: Vcm = 28.5V at 25C.

NOTES	RETS124AX REVISION 9A		TEST CONDITION UNLESS OTHERWISE SPECIFIED All voltages referenced to device ground.		TEST SYSTEM: DC PARAMETERS SBGRP 4 25 C		SBGRP 5 125 C		SBGRP 6 -55 C		DRIFT LIMITS 25 C	UNITS
	PARAMETER	SYM	V+	TEST #	min	max	min	max	min	max		
5	Large Signal Gain	Avs	15V	RL = 2K Ohms, Vo = 1V to 11V	50		25		25			V/mV
	Output Voltage High	Voh	30V	RL = 2K Ohms	26		26		26			V
			30V	RL = 10K Ohms	27		27		27			V
	Output Voltage Low	Vol	30V	RL = 10K Ohms		40		40		40		mV
			30V	Isink = 1 uA		40		100		100		mV
		Vol	5V	RL = 10K Ohms		20		20		20		mV

NOTE 5: Datalog reading in K = V/mV (for Teradyne program only).

RETS124AX DEVICE: LM124A FUNCTION: Low Power Quad Operational Amplifier

Appendix E. ENVIRONMENTAL TEST EQUIPMENT

Autoclave

The autoclave or "Pressure Cooker" test is performed using Express Test Model ET-242S vertical, fixed humidity (100%) steam pressure unit with a working temperature range of 100-133.0°C. The purpose of this test is to evaluate the moisture resistance (at saturation) and reliability of materials and processes used in the fabrication and packaging of integrated circuits. Corrosion of metallization affecting DC parameters and mobile ion charge effects are typical die related failure mechanisms resulting from autoclave exposure. Testing was conducted in accordance with JEDEC Std 22-B, Method A102-A. Temperature calibration in the autoclave chamber was completed to ensure 121°C test conditions. The supply water used in the autoclave chamber was 18 Meg-ohm DI water.

HAST

The highly accelerated stress test (HAST) or pressure, temperature, humidity, bias (PTHB) test is performed using Express Test Model HAST-1000 horizontal, variable humidity, dual vessel steam generator unit with a working temperature range of 100-160°C. The purpose of this test is to highly accelerate the unsaturated humidity testing of integrated circuits for process control and reliability assessment at a fraction of the time compared to using conventional humidity test equipment. Corrosion of biased metallization affecting the DC parameters from either moisture penetration and/or mobile ions are typical die related failure mechanisms. Testing was conducted in accordance with JEDEC Std. No. 22, Method A110. A 15 point data aquisition system was incorporated into the chamber to provide online monitoring / profiling of the temperature within the test chamber during operation. This temperature data was plotted and recorded. The supply water used in the autoclave chamber was 18 Meg-ohm DI water.

Temperature Cycling

Temperature cycling testing is performed using Thermotron Model ATS-195V-5-5-LN2 vertical, air to air thermal shock unit with a working temperature range of -73 to +200°C. The purpose of this test is to assess the material compatibility and resistance

of a device to alternate accelerated exposures of high and low temperatures. Cracking and eventual breakage of the die, interconnect, and package (or protective coating) are typical failure mechanisms. Testing was conducted in accordance with MIL-STD-883D, Method 1010.7, test condition C. The temperature recovery time for the standard 1.0 pound piece of steel was 5 minutes. Calibration of the chamber temperature was within 1°C in the hot zone at +150°C and within 2°C in the cold zone at -65°C. Test temperature conditions were plotted and recorded.

Salt Fog

Salt fog testing is performed using Associated Environmental Systems Model MX-9204 bench top salt spray chamber. The purpose of this test is to assess the materials resistance to accelerated laboratory corrosion simulating the effects of seacoast atmosphere on devices and package elements. Testing was conducted in accordance with MIL-STD-883D, Method 1009.8, test condition A. Recording of required data for the initial salt solution, uniformity of fog, and collected salt solution was completed. The devices were mounted on polytetrafluoroethylene (PTFE) fixtures designed to provide a 15° incline from the normal during exposure.